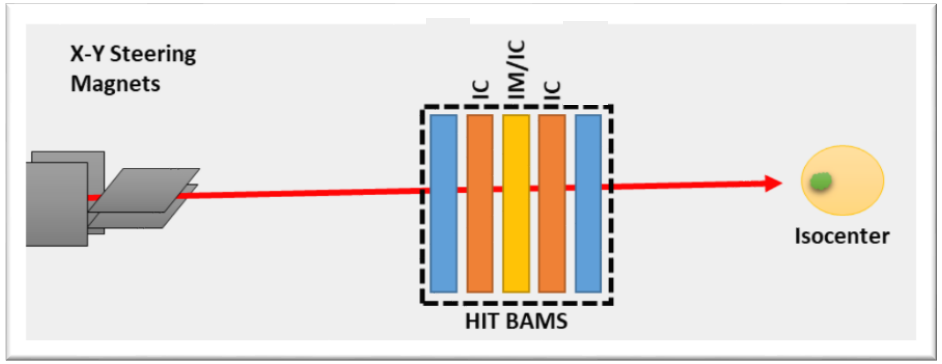
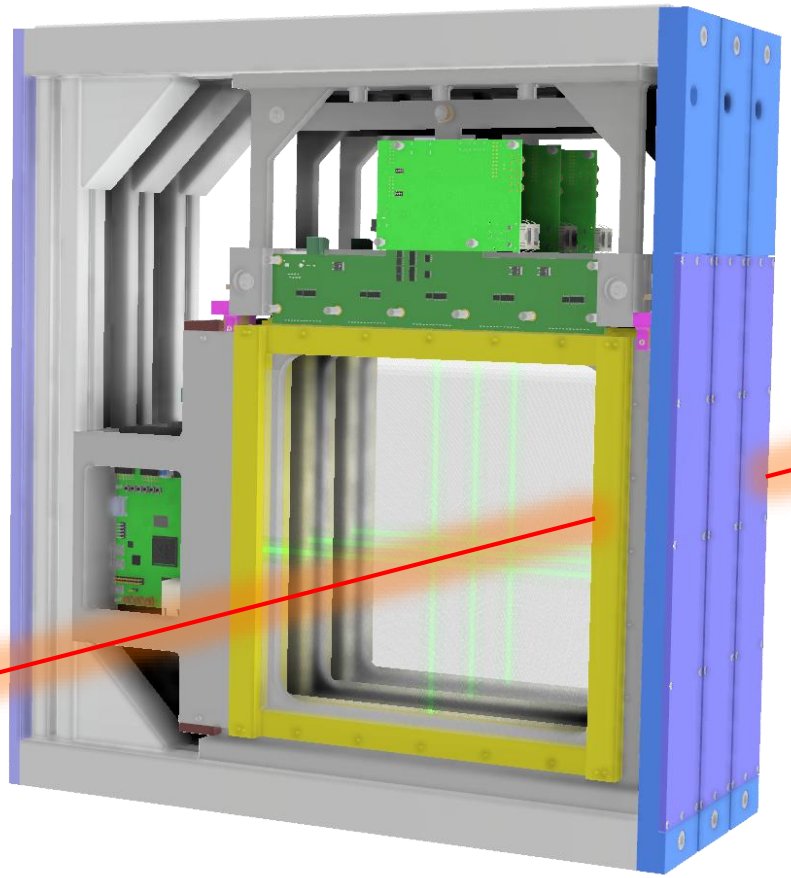
The Electronics of the Scintillating Fibre Beam Profile Monitor for Ion Therapy Beams

Blake Leverington, Liqing Qin, Michael Dziewiecki*

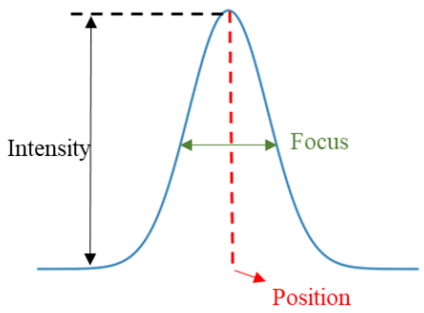


DFG Deutsche Forschungsgemeinschaft

Beam monitor for raster-scanning



2023 engineering prototype



Sketch for beam profile.

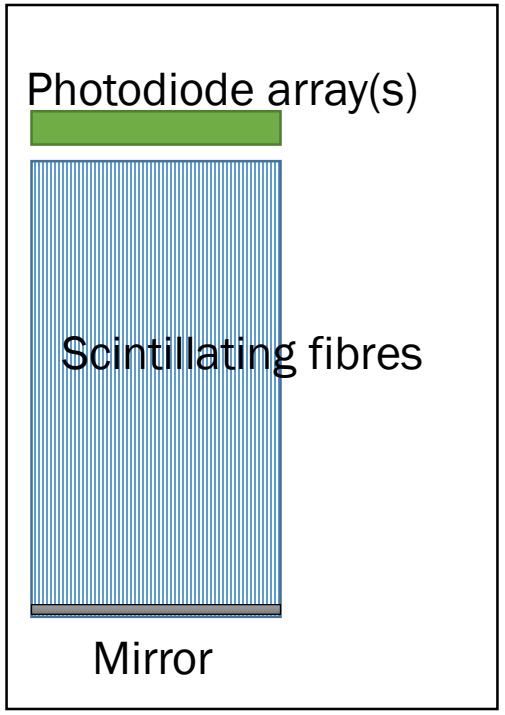
Parameter	Steps	Protons	Carbon
Energy	255	48 - 221 MeV/u	88 - 430 MeV/u
Penetration	255	20 - 300 mm	20 - 300 mm
Intensity	9	$8 \times 10^7 - 2 \times 10^9 s^{-1}$	$2 \times 10^6 - 8 \times 10^7 s^{-1}$
Beam Size	4	8 - 20 mm	4 - 12 mm

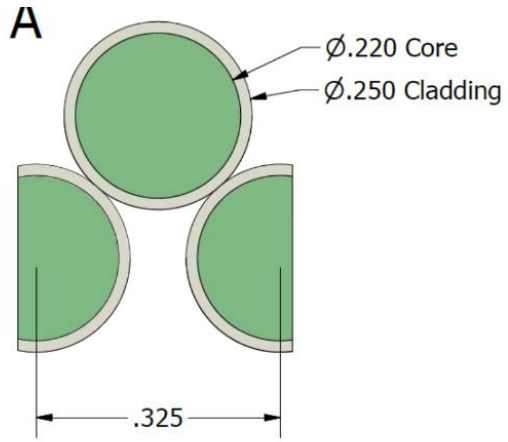
Prompt feedback of the beam position
- Interlocks for patient safety
- Feedback loops for position correction

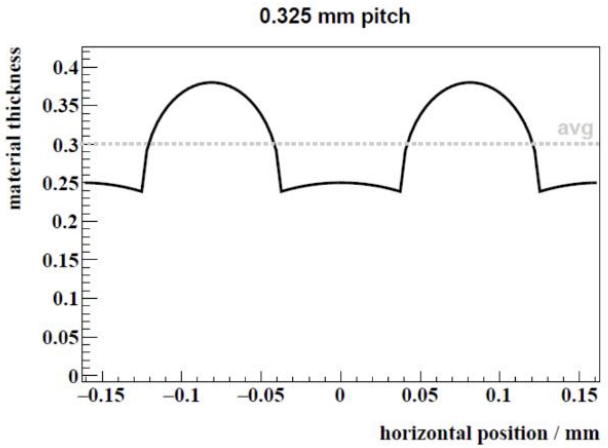
- Replacement of the MWPCs currently used requires
  - >4 to 8 kHz readout
  - Light (<0.3mm Water Eq. per plane)
  - 0.2 (0.4) mm position (FWHM) resolution

2-layer glueless* mats

*Glueless in the acceptance but glued at the ends

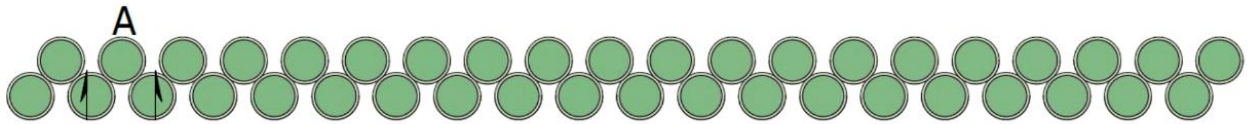


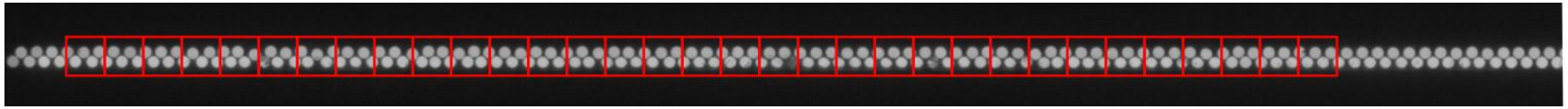




0.3mm of material on average

Green SCSF-3HF from Kuraray
to be more “radiation hard”

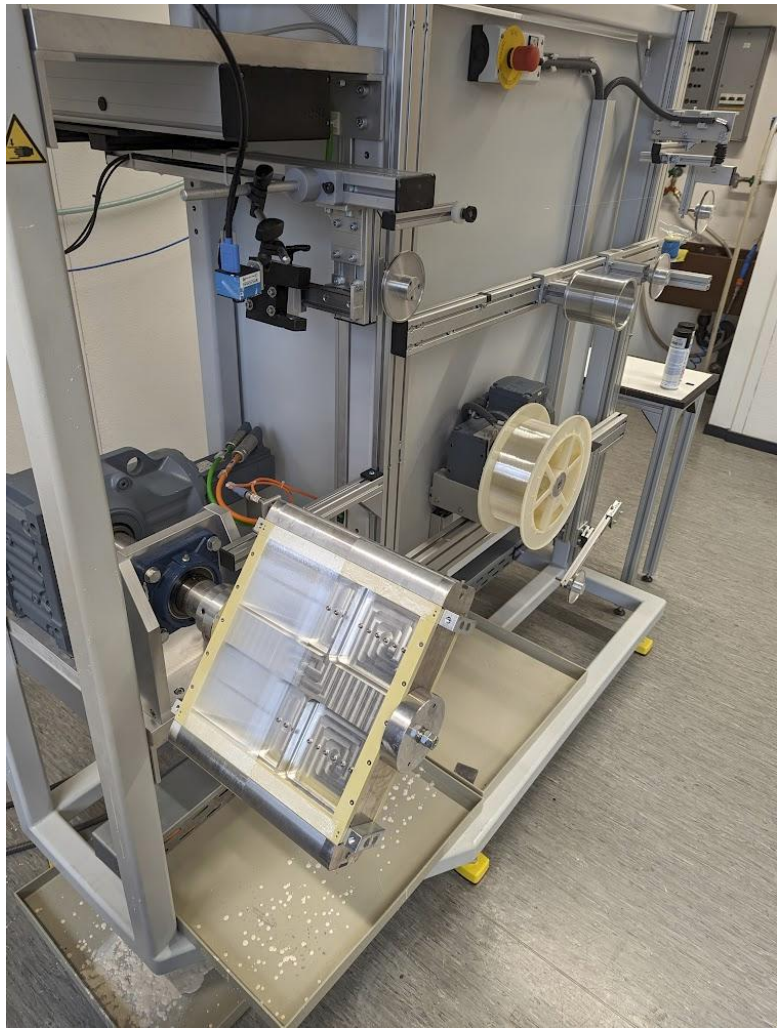


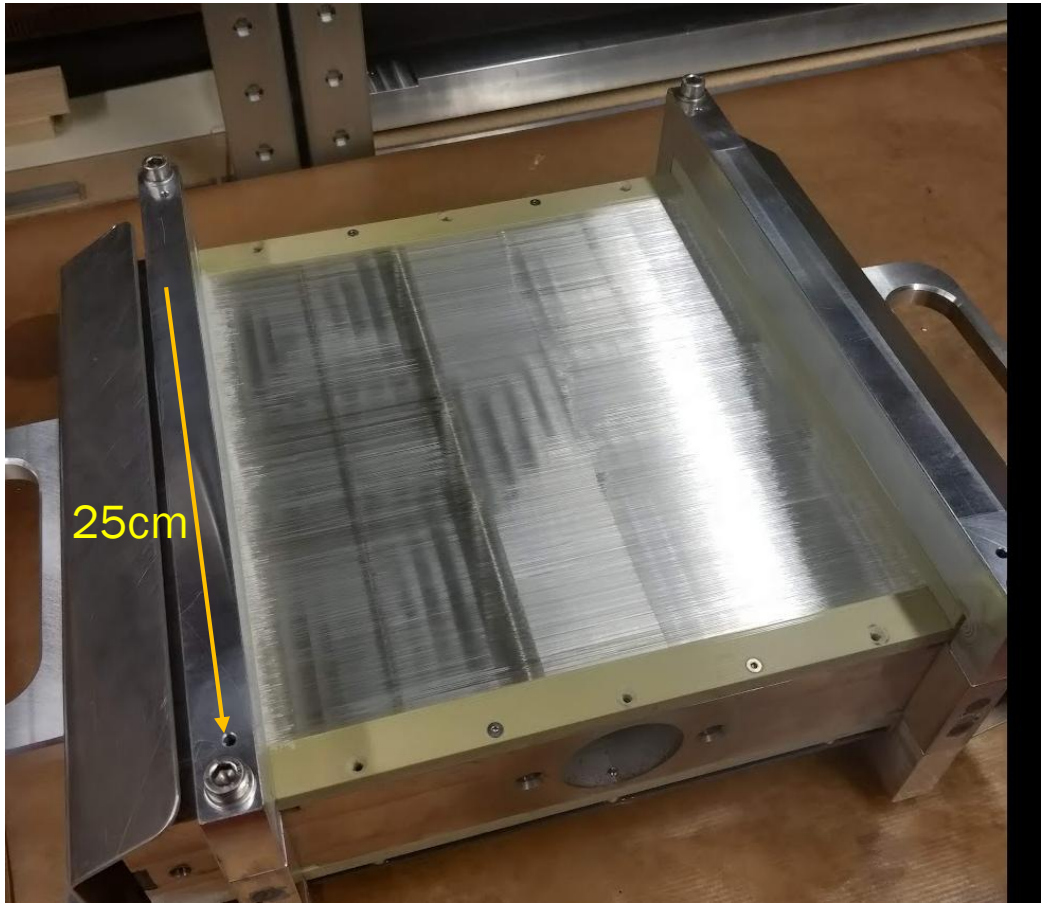


Scan of 1 fibre plane end

Photodiode pitch: 0.8 mm

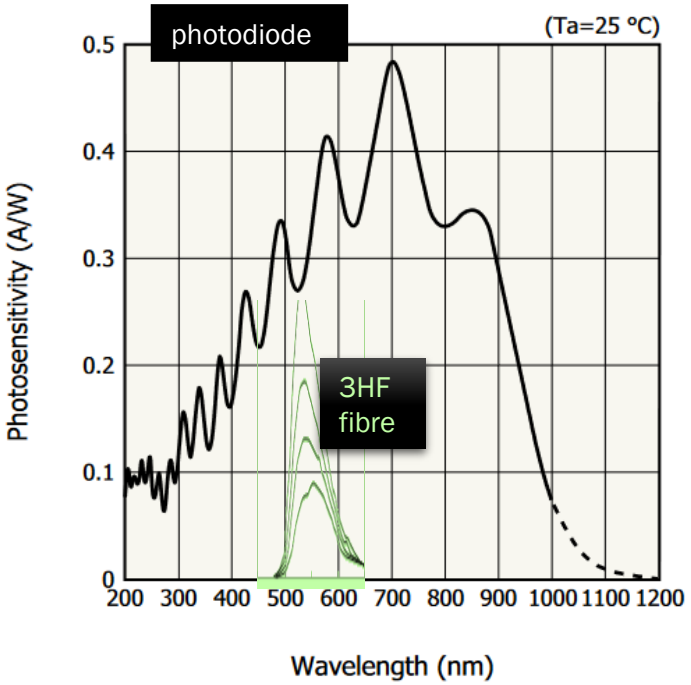
Winding on the LHCb Machine

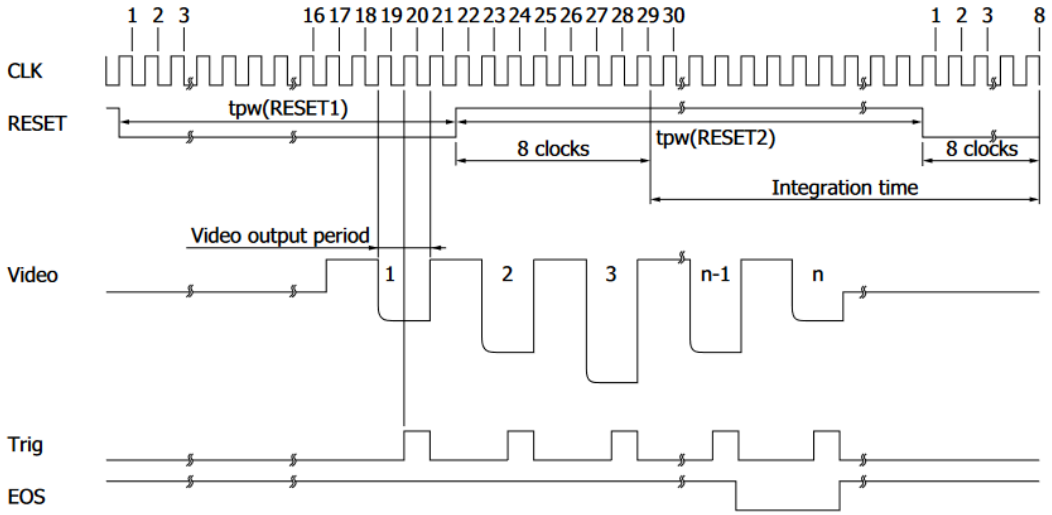




5 Photodiode arrays

25cm





Measure with an ADC (3.57 MHz clock)

10 kHz full frame readout (adjustable for longer integration times)

Photodiode Arrays

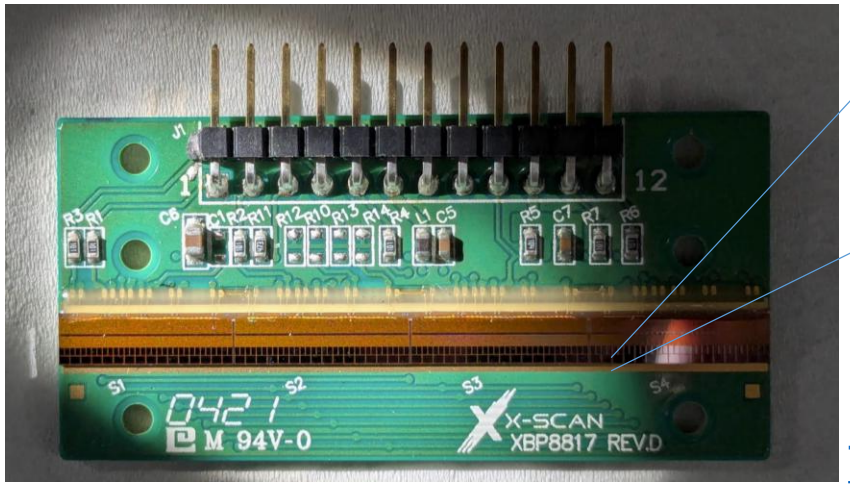
Image size	51.2 x 0.8 mm
Number of effective pixels	64 pixels
Pixel size	0.7 x 0.8 mm
Pixel pitch	0.8 mm
Supply voltage	5 V
Scintillator	None
Spectral response range	200 to 1000 nm
Peak sensitivity wavelength	720 nm
Line rate max.	14678 lines/s
Charge amp feedback capacitance	0.5 pF

0.7 x 0.8 mm

Tech. Doc

Same clock and reference voltage pins;

Parameter	Symbol[i]	XB8804R-2.0[ii] (low resolution 0.8-mm mode)[iii]	XB8804R-2.0 (high resolution 0.4-mm mode)[iv]
Element pitch	P	0.8	0.4
Element diffusion width	W	0.76	0.36
Element height	H	1.2	0.6
Number of elements	–	64	128
Active area length	–	51.2	51.2



0.76 x 1.2 mm

Tech. Doc.

Photodiode Pinout

S11865-64/-128, S11866-64-02/-128-02

Pin no.	Symbol	Name	Note
1	RESET	Reset pulse	Pulse input
2	CLK	Clock pulse	Pulse input
3	Trig	Trigger pulse	Positive-going pulse output
4	EXTSP	External start pulse	Pulse input
5	Vms	Master/slave selection supply voltage	Voltage input
6	Vdd	Supply voltage	Voltage input
7	GND	Ground	
8	EOS	End of scan	Negative-going pulse output
9	Video	Video output	Negative-going output with re
10	Vref	Reference voltage	Voltage input
11	Vgain	Gain selection terminal voltage	Voltage input
12	Vpd	Photodiode voltage	Voltage input

XB8804R-2.0)

■ **Pin connections**

Pin No.	Symbol	Name	Description
1	RESET	Reset Pulse	Negative-going pulse input
2	CLK	Clock Pulse	Pulse input
3	TRIG	Trigger Pulse	Positive-going pulse output
4	EXTSP	External Start Pulse	Pulse/voltage input
5	VMS	Master/Slave Selection Voltage	Voltage input: See Master/slave selection voltage VMS and external start pulse EXTSP settings note
6	VDD	Supply Voltage	5-V supply voltage
7	GND	Ground	Common ground voltage
8	EOS	End of Scan	Negative-going pulse output
9	VIDEO	Video Output	Negative-going output with respect to VREF
10	VREF	Reference Voltage	Voltage input
11	SNS	Sensitivity Selection	Voltage input: High (VDD) for high sensitivity (Cfhs) Low (GND) for low sensitivity (Cfls)
12	RS	Resolution Selection	Voltage input: (Disabled for 0.8mm mode only; don't care) High (VDD) for 0.4-mm pitch Low (GND) for 0.8-mm pitch

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Electronics Concept

Each of the 5 sensors (Hamamatsu S11865-64) is an array of 64 photodiodes with an integration/readout circuit (IC).

The IC allows simultaneous integration of photodiode currents for some period sends it out as a series of voltage pulses over a single wire.

To perform this, it needs some constant-level signals:
- a clean power supply of 5V
- an extremely clean reference voltage of 4.5V (nom.)
- a photodiode bias voltage (essentially, the same signal as above)

Further, it needs two digital waveforms:
- a clock, which should be no more than 4 MHz
- an integration window signal (called RESET by Hamamatsu, don't ask why…)

Having these signals, it will produce the output signals:
- the Video signal – a series of analog pulses referred to the reference voltage (mentioned above) with negative polarity
- the Trig and EOS signals, which we don't use.

Electronics Concept: ADC Board + FPGA Board

- Produce a valid clock signal
- Produce a valid Reset signal
- Collect Video pulses at right times and ADC them.

Again, an ADC (with an SPI interface) needs its own reference, clock and trigger, and a data line.

At the end, we should have 5 · 64 samples of sensor data somewhere in our memory.
Now we can pack these data into a UDP packet and send it over Ethernet to a PC.

Simple? Not really. If we have multiple boards, we need to *synchronize* them. This is done by a synchronization link on two levels:

– ***frame-level synchronization (same frame counter, 3.57 MHz sensor clock)***,
– ***fine synchronization (***50 MHz oscillator on each board, ***rising edge within ~20ns)***
– we synchronize the sensor clock to our “master board” trigger to maintain alignment precision

– Can inject an external 8-bit digital signal in each frame for synchronization with external systems (“time stamps”

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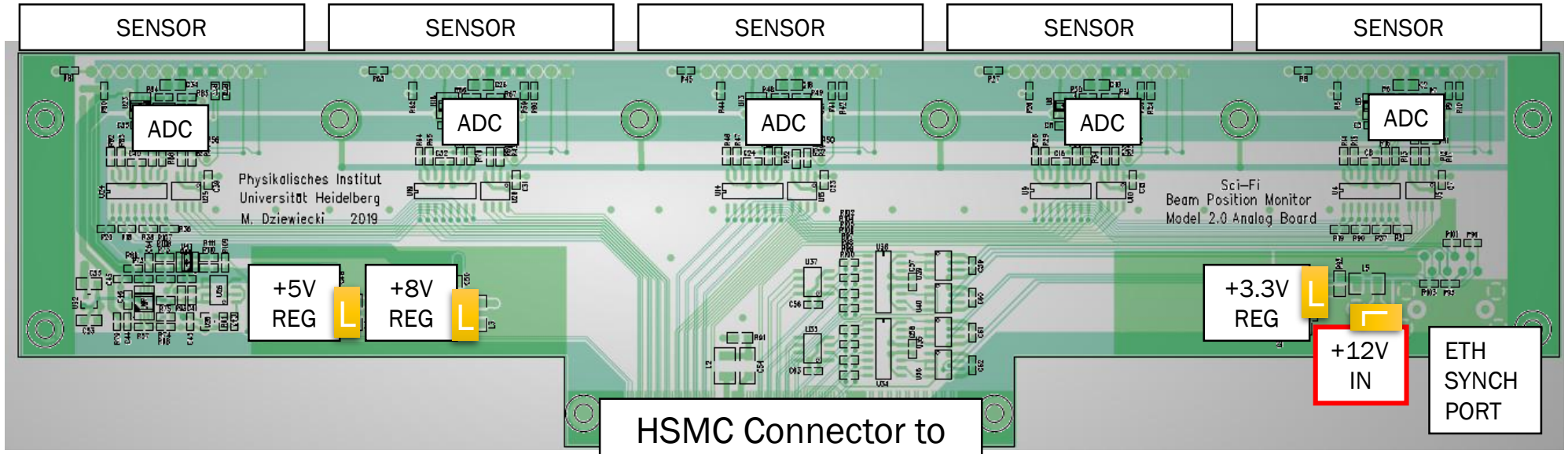
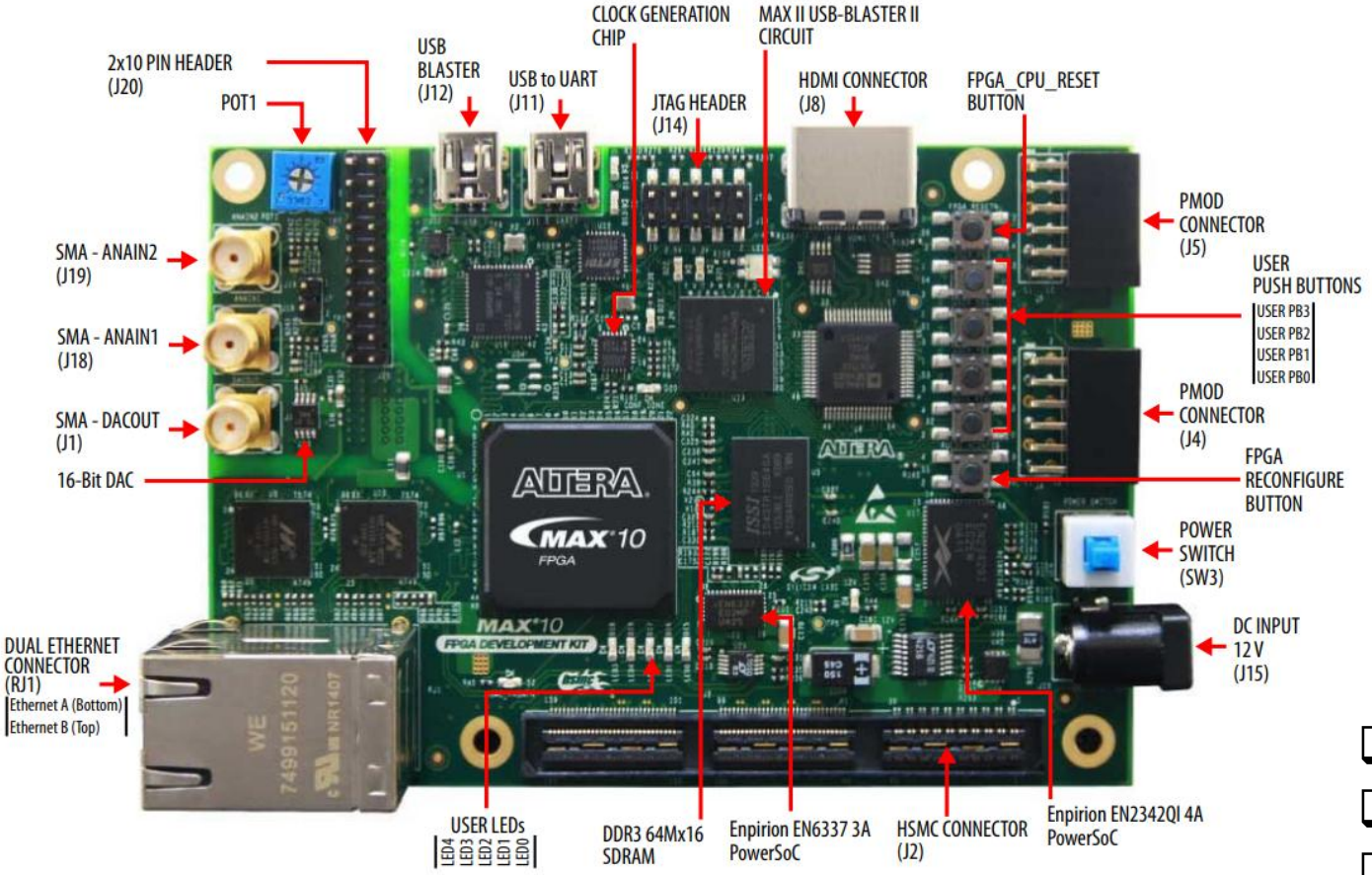
Beam Position Monitor
Technical description

Author(s): Michał Dziewiecki
Document revision: 1.0 (issue 1)
Hardware version: 1+2, mainly 2

ADC Sensor Board

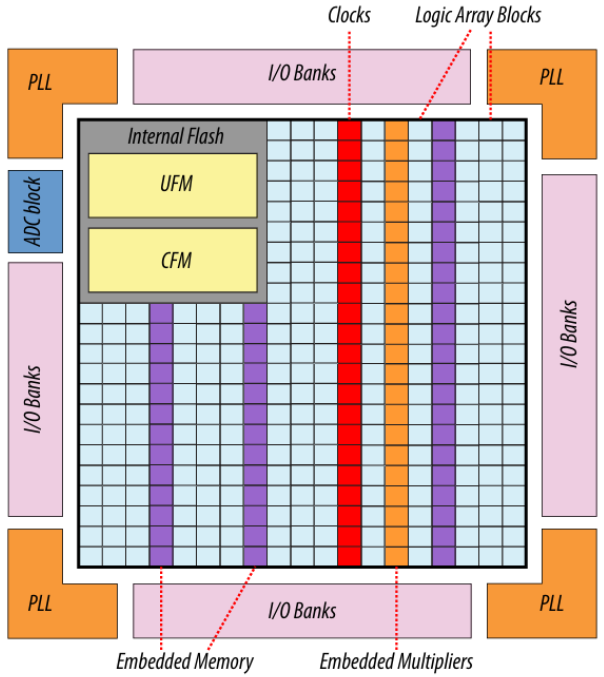


ALTERA MAX10 Development Board



MAX10 Development Board

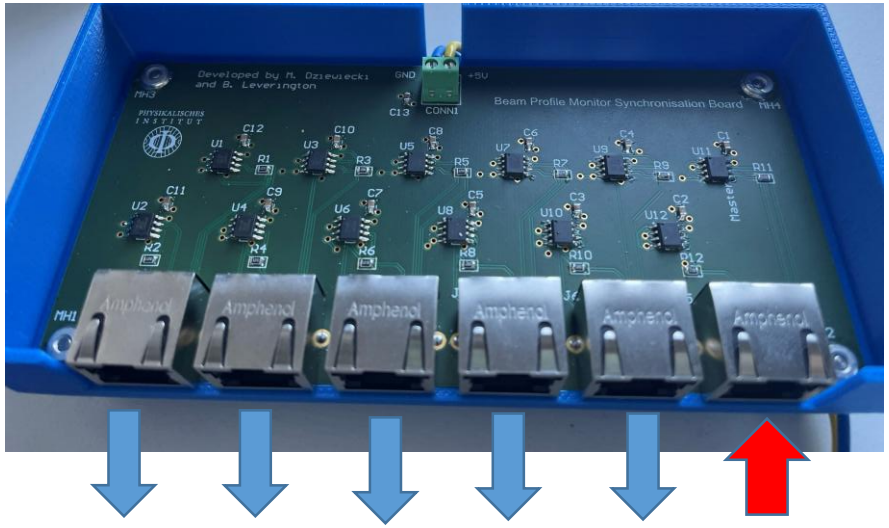
Needs terminating resistors for LVDS receivers added



MAX10 FPGAs

- HSMC Connector: connect with ADC board
- MAX10 FPGAs: CPU, Data Processing
- Ethernet Connector: communication
- DDR3: RAM for Software
- Flash: for store FPGAs image
- Power

Synchro Board



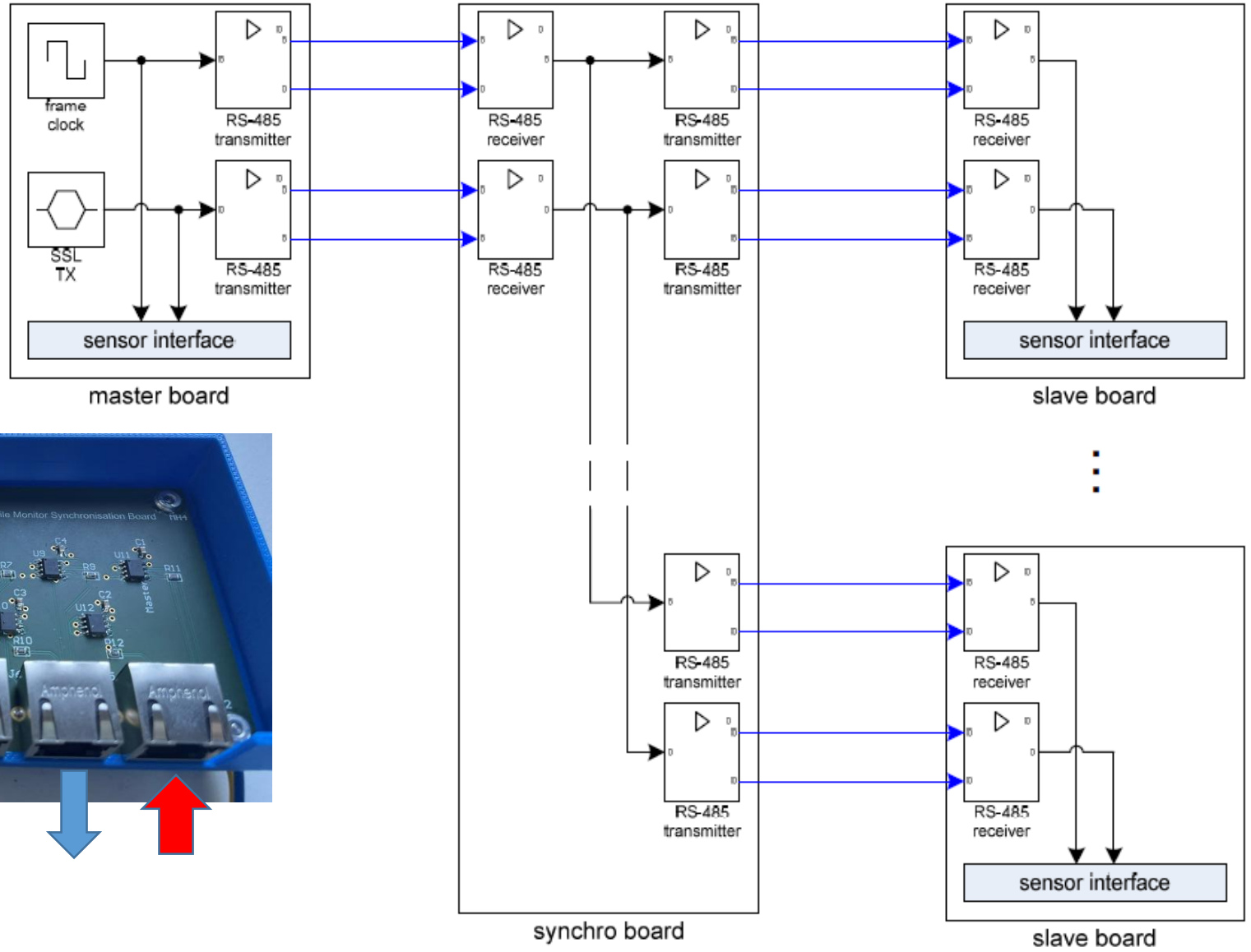


Fig. 2-21 Simplified diagram of the synchronization system. SSL TX is the transmitter for synchronization serial link. RS-485 pairs are shown in blue. Debouncers are omitted.

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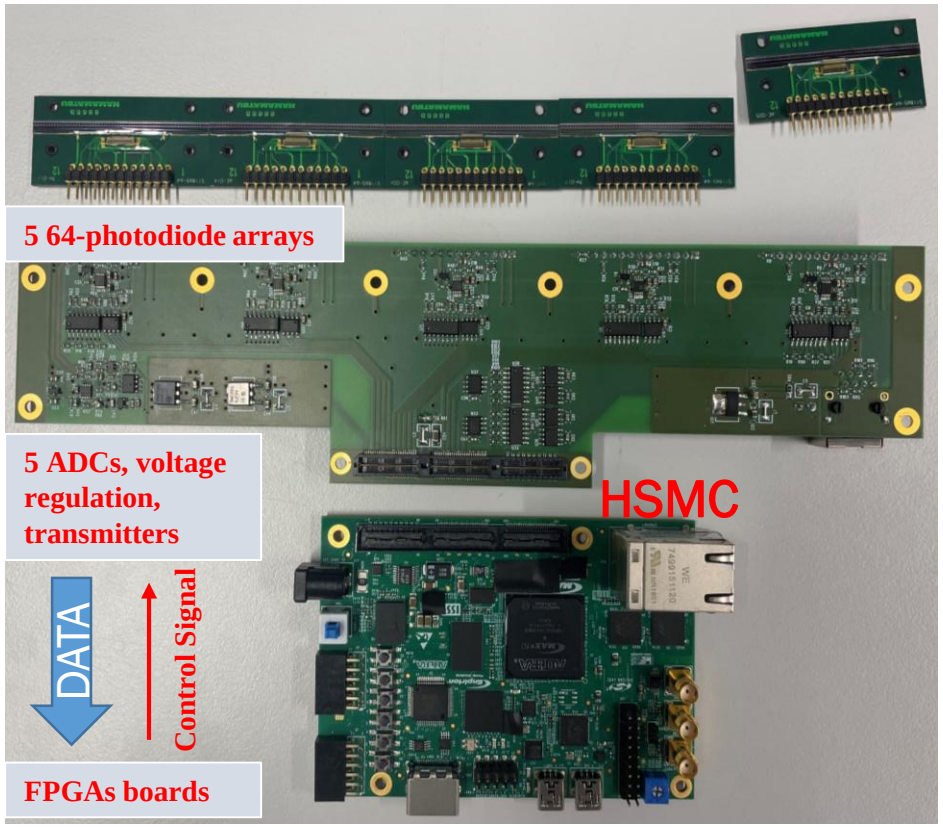
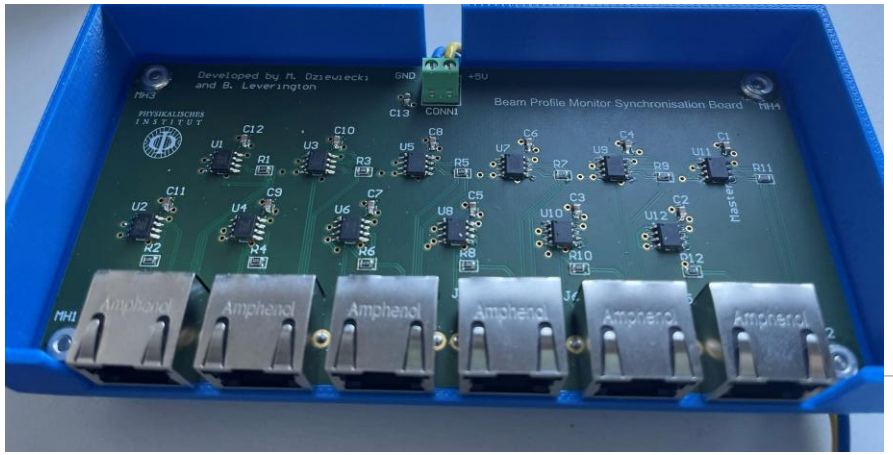
Electronics



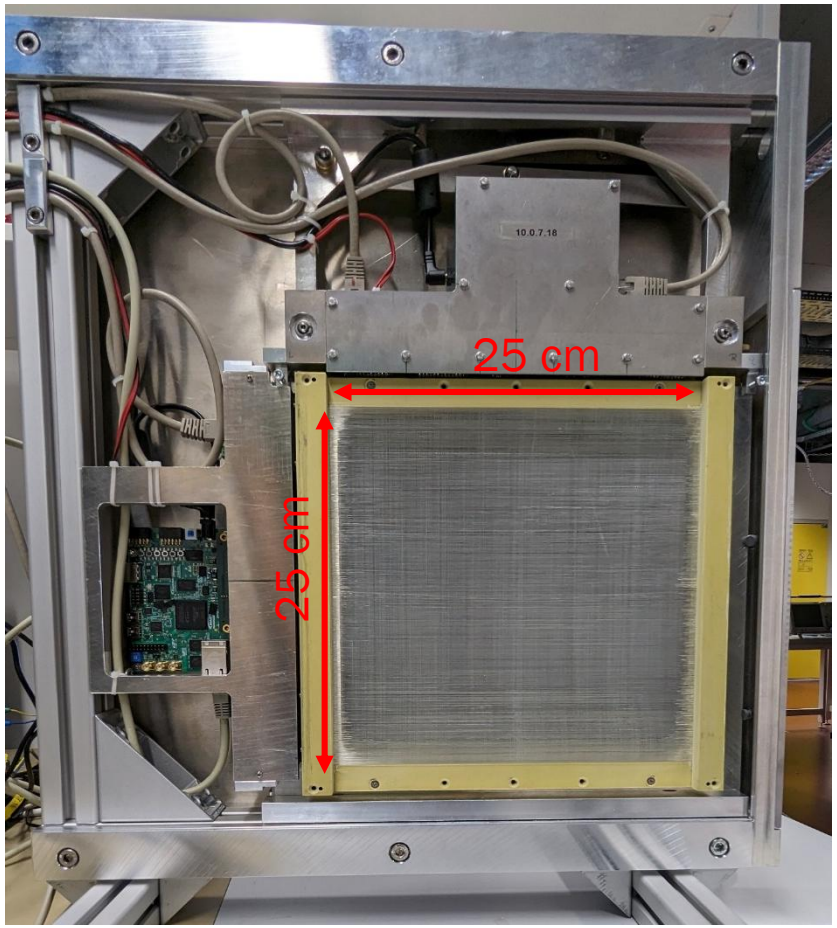
12V Power supply for ADCs board, can support 3 XY stations

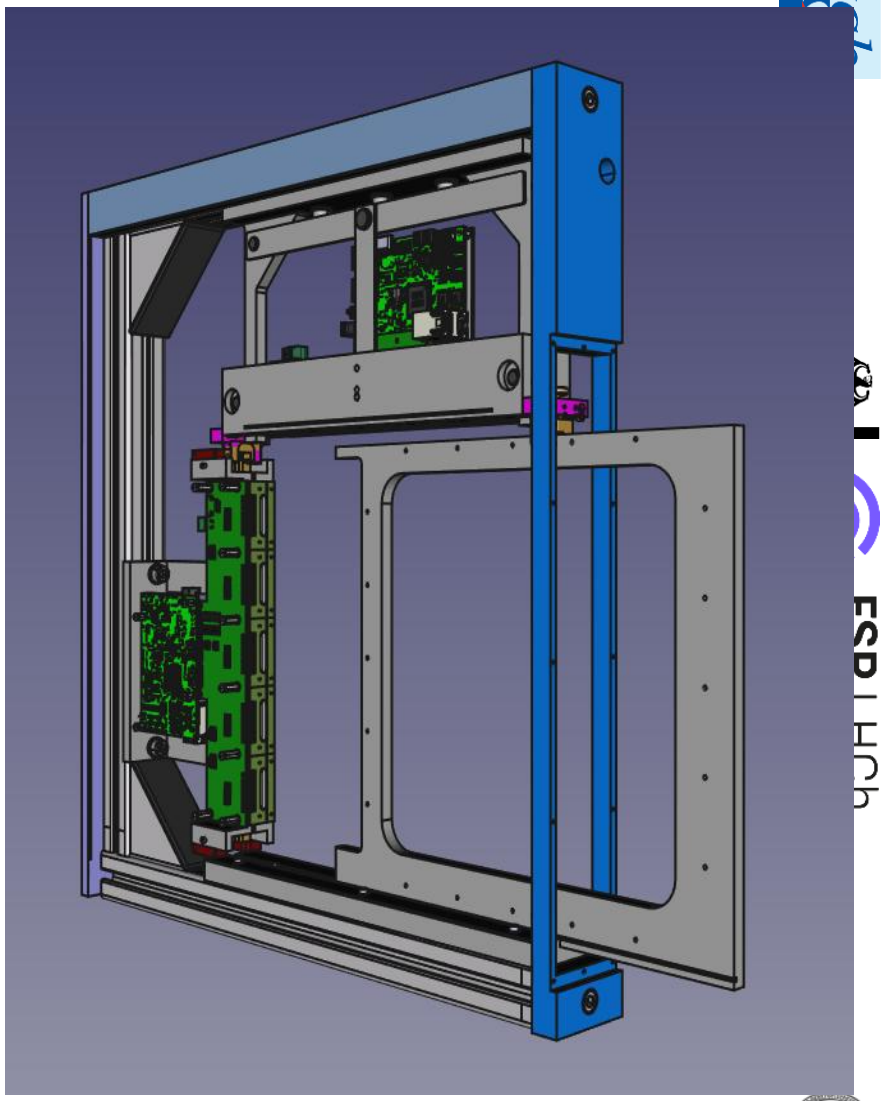
ADCs board: provide voltage for ADCs and sensors, bridge signals and hold 5 ADCs

MAX10 FPGA board controls photodiodes arrays and ADCs, collects signal from all the channels, reconstructs position and sigma, packs data into UDP package, sends to internet.

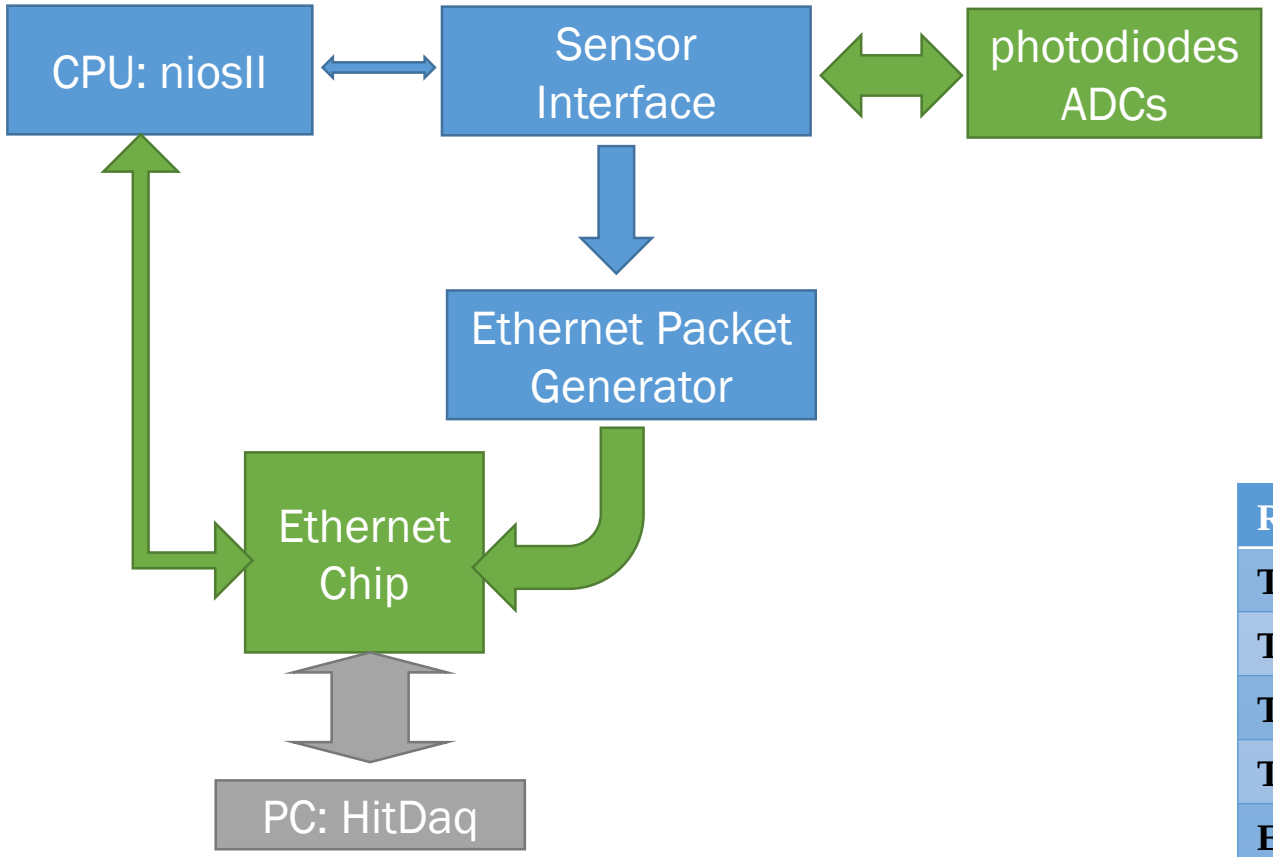


Synchronization board receives the sync signal from master board and broadcasts to slave boards.


25 cm
25 cm



Readout

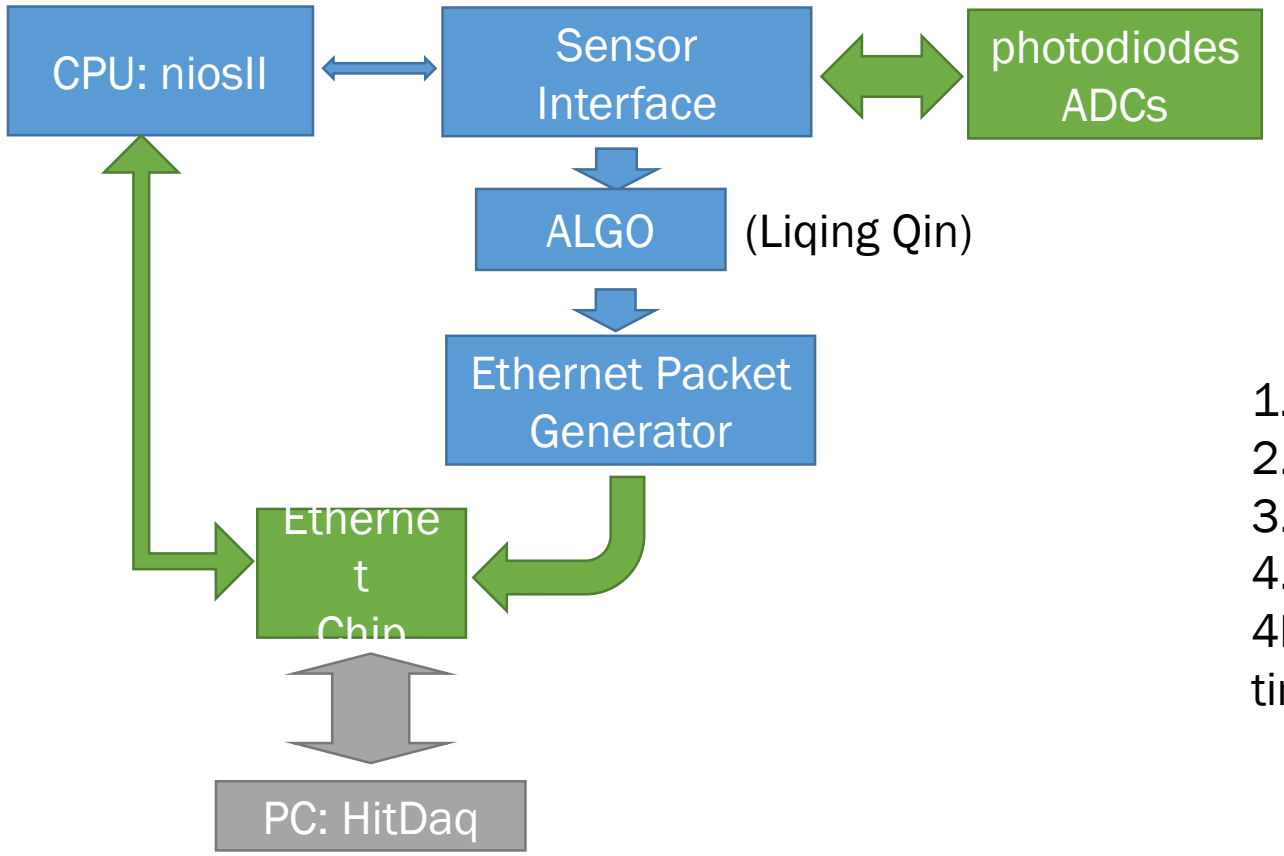


Simplified diagram for the readout HIT Beam Profile Monitor
Blue parts are on the MAX10 FPGA

- CPU sets up socket server
- FPGAs and PC talk through ethernet
- The sensor interface controls Photodiode arrays and ADC, collect and send data to Ethernet Packet generator and then to Ethernet.

Resource on Max10	Usage
Total logic elements	32,471 / 49,760 (65%)
Total registers	23632
Total pins	156/360 (43%)
Total memory bits	284,392 / 1,677,312 (17%)
Embedded Multiplier 9-bit elements	6 / 288 (2%)
Total PLLs	2 / 4 (50%)

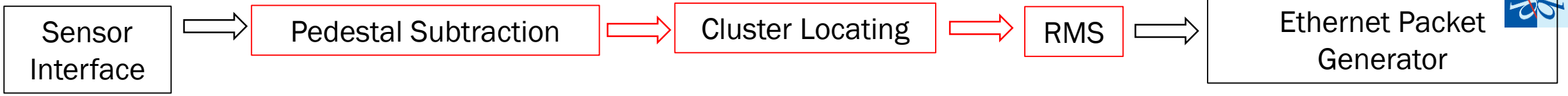
Add ALGO for beam reconstruction



1. Background noise subtraction
2. Calibration parameters per channels
3. Thresholds & Selection
4. RMS for mean and width

4b. Not enough logic elements (person time) for Linear Regression

ALGO Current Status



Due to the limited logic resource on Max10, and tolerance in latency:

- Calculation is done one channel by one channel;
- RAMs are used for store the pedestal;
- All the calculations are with fixed point;

The size of each registers is from C++ code simulation.

From the end of integration window for photodiodes, until the result stream out, there is about 94 microsecond latency (about **8 microsecond** from calculation);

calculation and data transfer within 100 microseconds

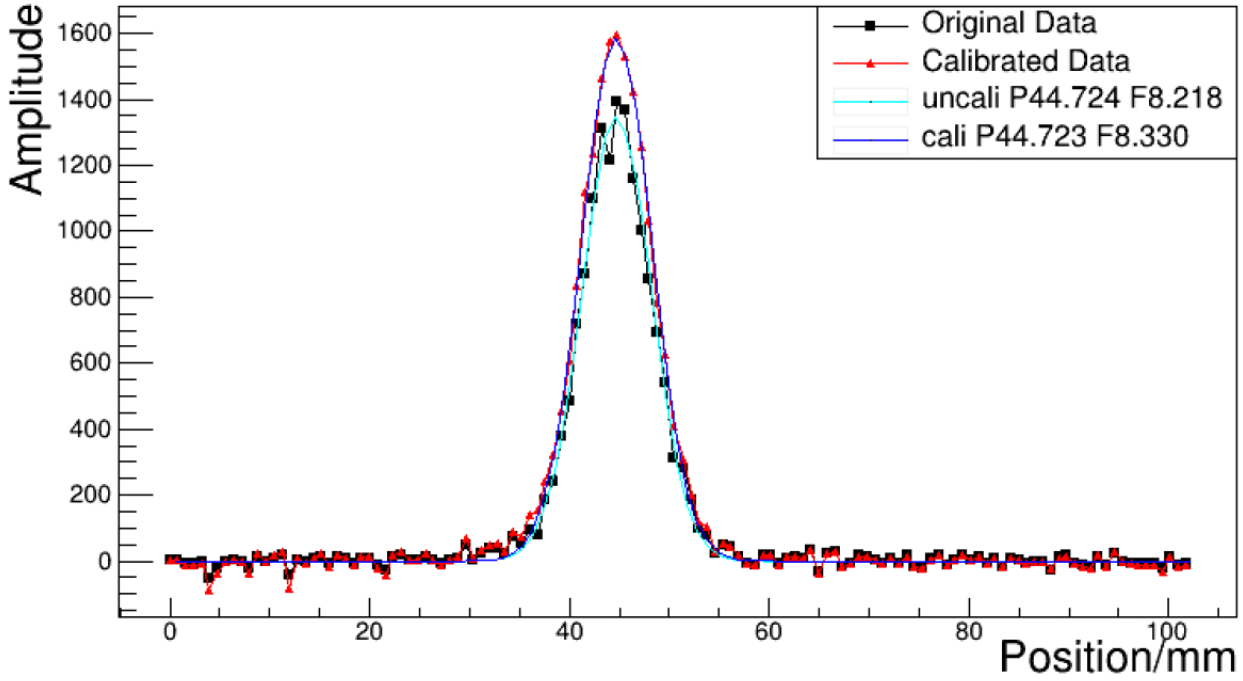
Resource on Max10	usage
Total logic elements	36,421 / 49,760 (73%) +8%
Total registers	26547 +2915
Total pins	156/360 (43%)
Total memory bits	307,750 / 1,677,312 (18%) +1%
Embedded Multiplier 9-bit elements	14 / 288 (5%) +3%
Total PLLs	2 / 4 (50%)

Num	RegisterName	bitsize
0	X.Max	11
1	Y.Max	15
2	Y.Sum	18
3	XY.Max	27
4	XY.Sum	29
5	MeanXleftshift	13
6	DiffxMeanX.Max	13
7	DiffxMeanX2.Max	26
8	DiffxMeanX2Yi.Max	41
9	DiffxMeanX2Yi.Sum	38
10	Sigma2	26
11	Sigma0	11

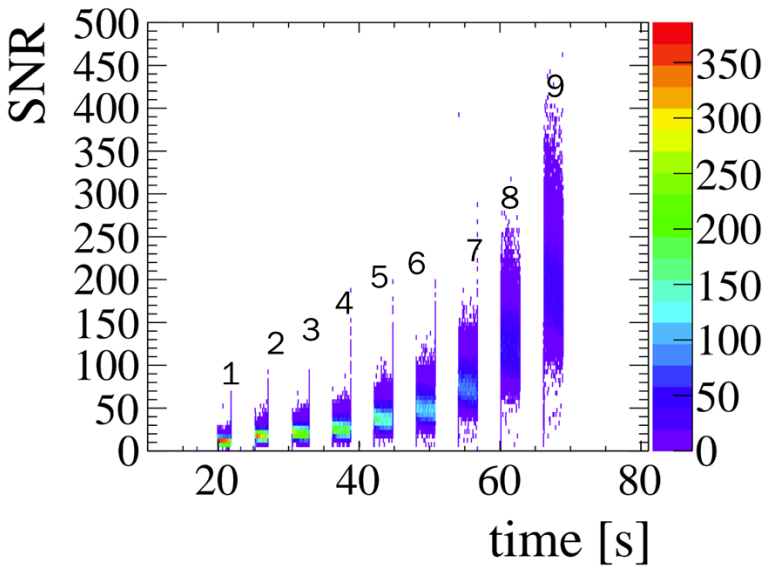
Registers list for RMS example.(the size on FPGA is larger than the bitsize in the table)

Signals

221 MeV Proton Beam at the iso-centre



Original signal vs. calibrated signal for detection plane 3. Proton 221.06 MeV 8.1 mm 2 · 10^9/s



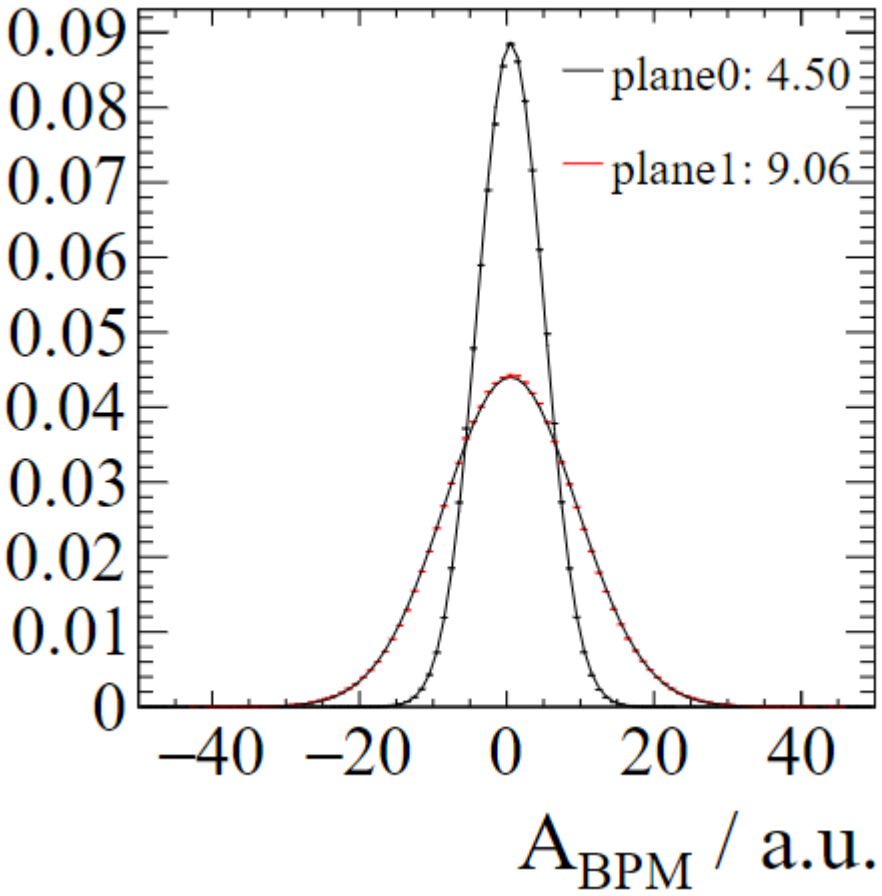
Intensity Setting	10^6 s^{-1}
1	80
2	120
3	200
4	320
5	400
6	600
7	800
8	1200
9	2000

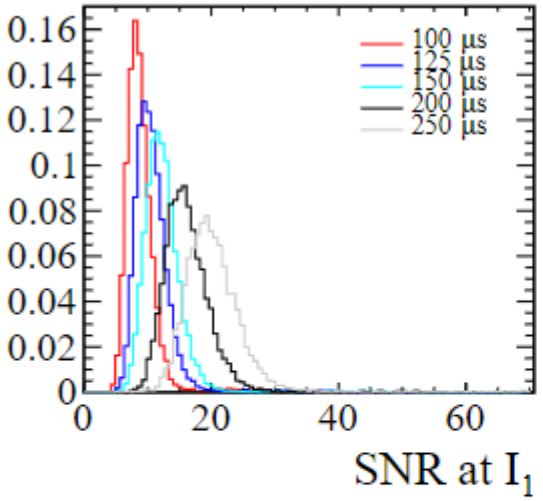
Factor of 25 range in intensity

At the vacuum window, the beam is ~2mm FWHM

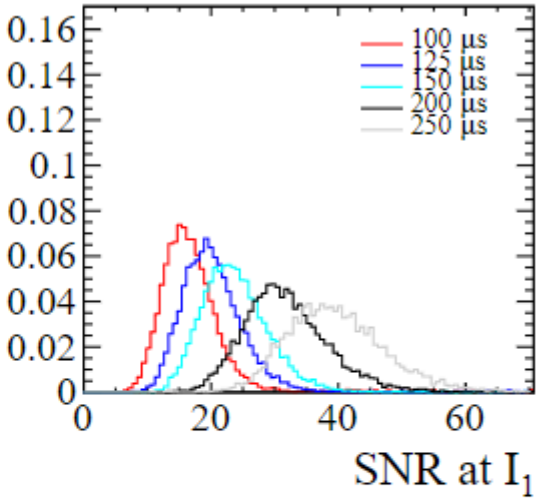
Noise and SNR

Optimisation of noise is important. We see some common mode noise on a couple boards. To be debugged. Could be the voltage regulators or the Ferrite beads are the wrong value.





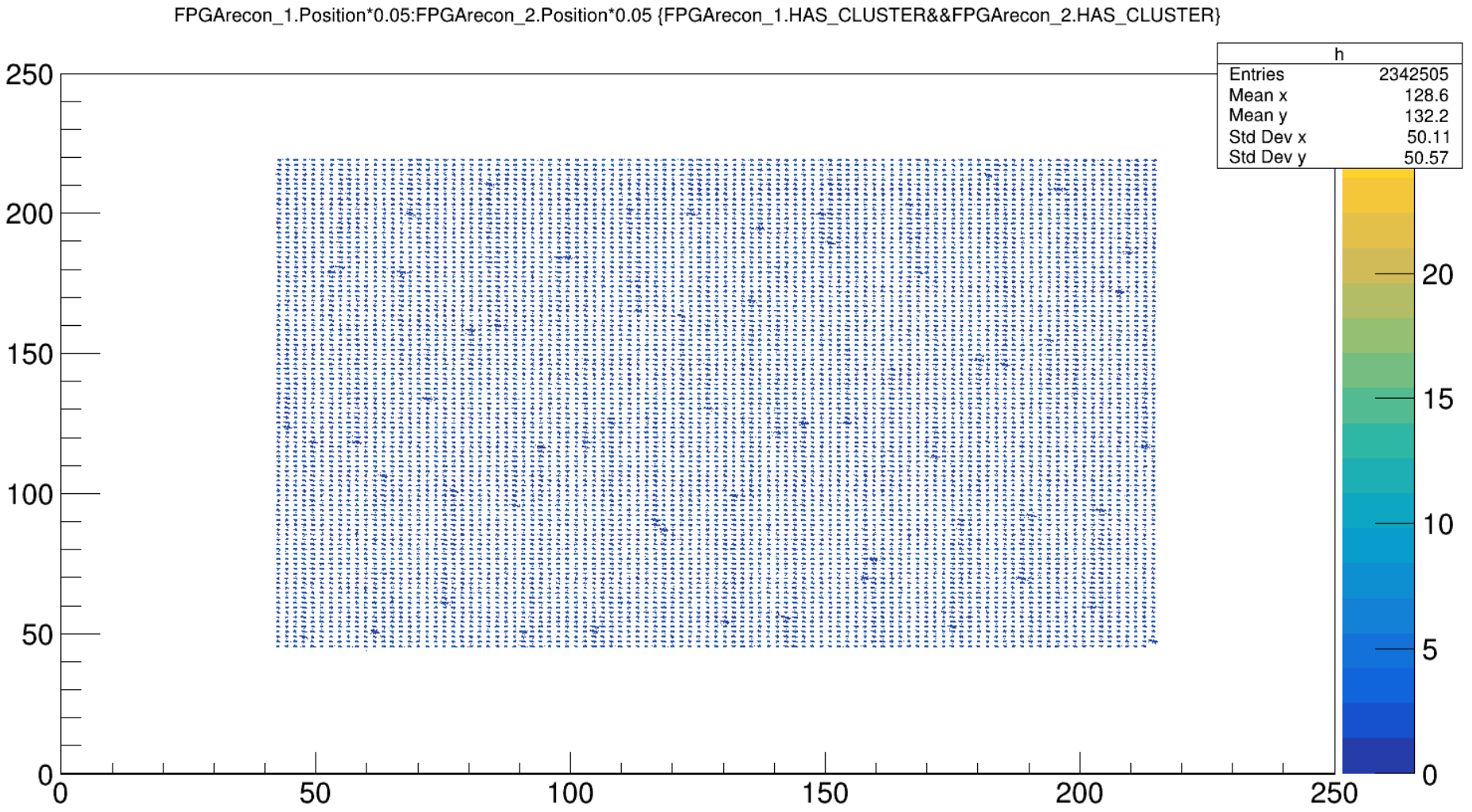
(A) Plane 0



(B) Plane 1

FIGURE 6.7: The normalized histograms of SNR with different integration time at the lowest intensity setting I_1. The beam setting: an 8.1 mm wide 221 MeV proton beam at a fixed position with intensity I_1 $8 \times 10^7 s^{-1}$.

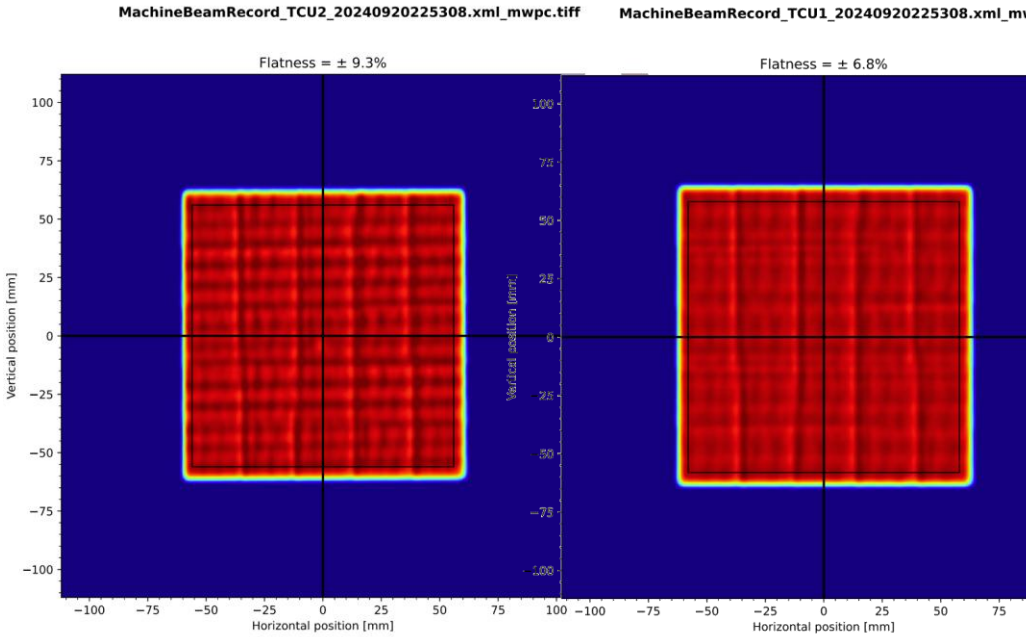
Uniform Field Scan



Uniform Field Scan*

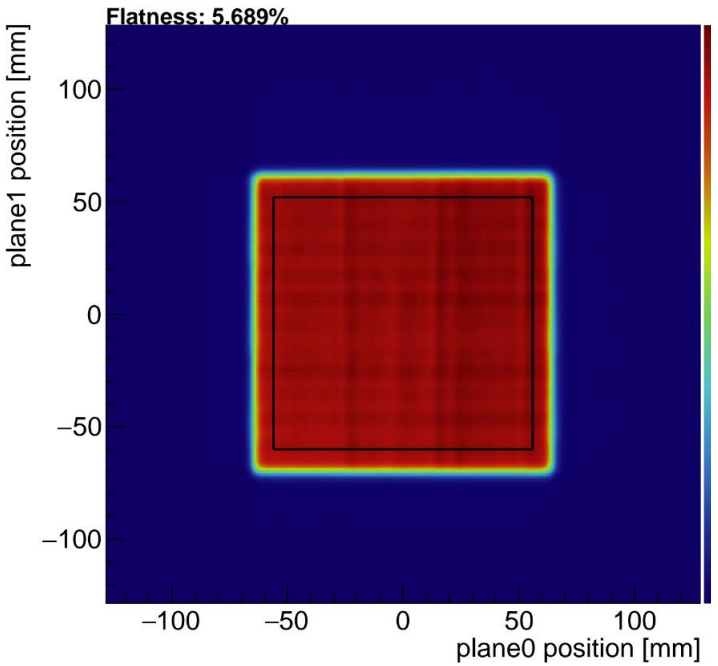
*MWPC Position Feedback-loop enabled in this data

MWPC assumes a gaussian shape (pos, width). Fibre = amp(X_i) *amp(Y_i) from raw per channel data.

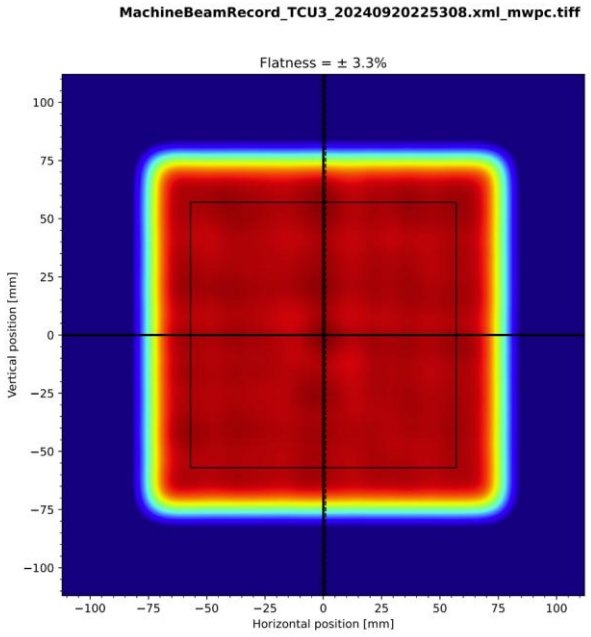


M_1 (MWPC)

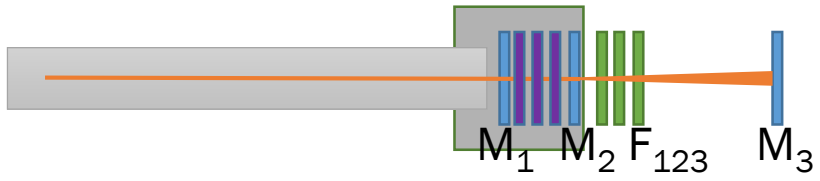
M_2 (MWPC)

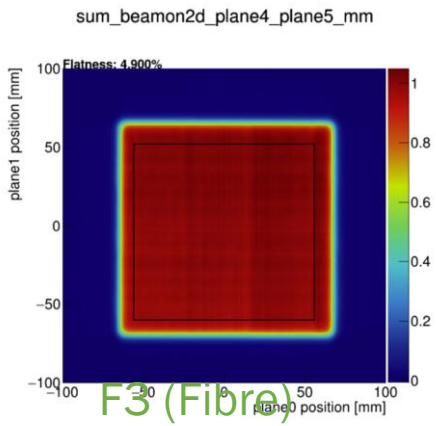


F1 (Fibre)



M_3 (MWPC)

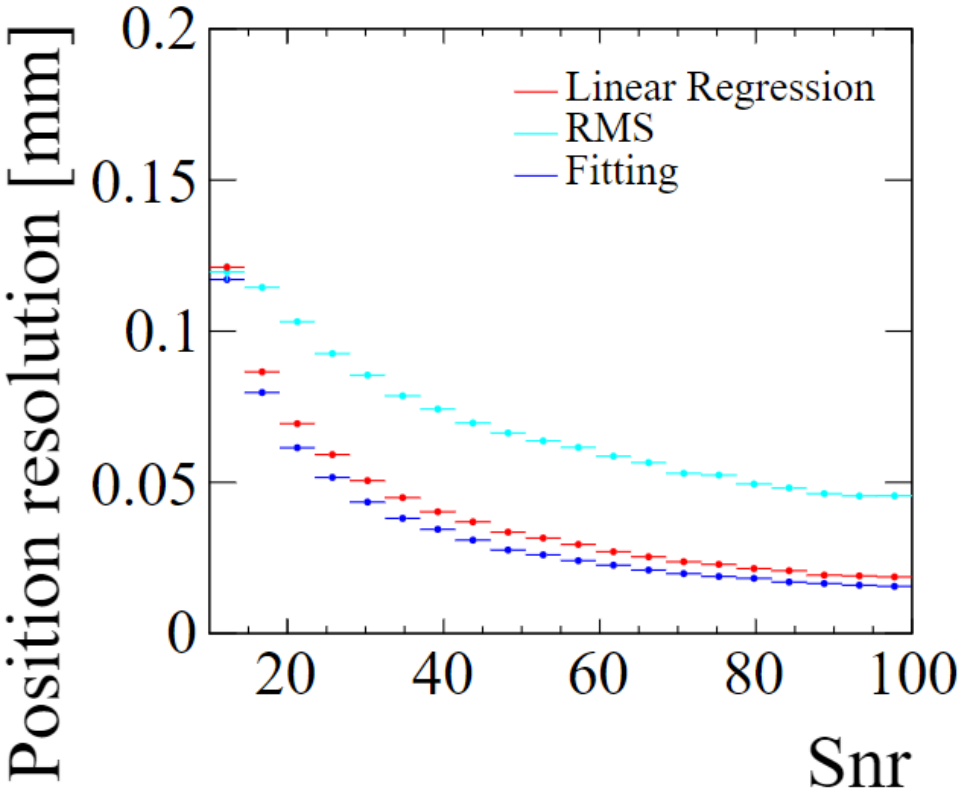




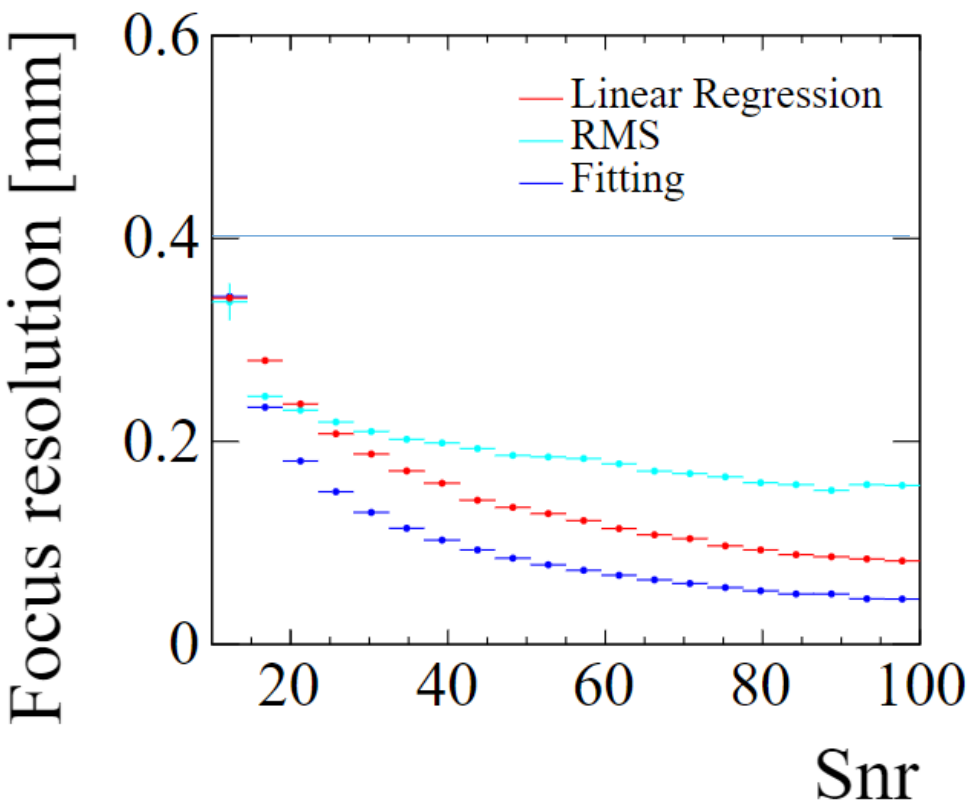
F3 (Fibre)

BPM Performance

RMS is currently performed directly on the FPGA (PhD work of Liqing Qin)



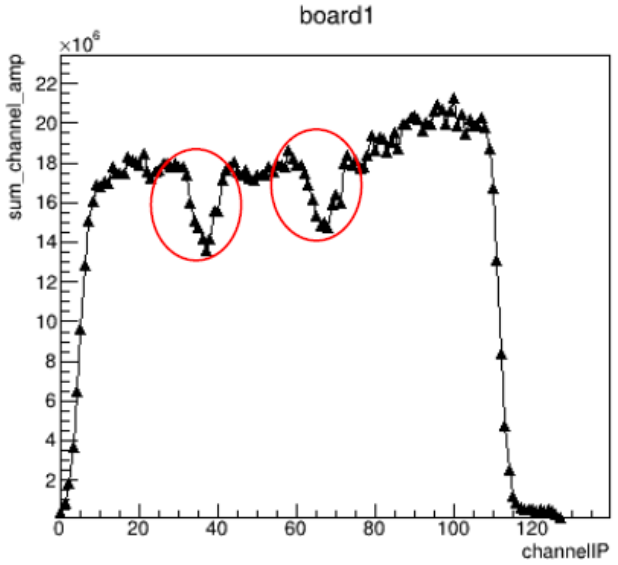
"Focus" = FWHM



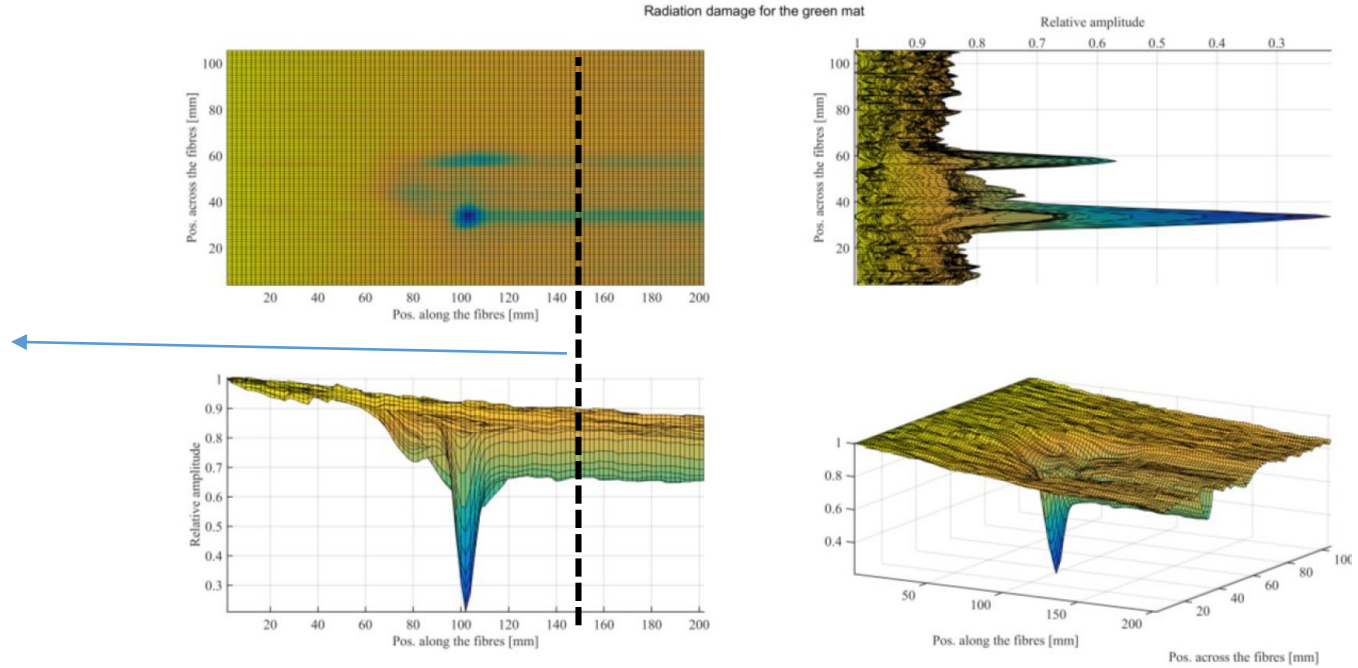
Here, the width of the residual / sqrt(2) between two neighbouring stations is taken for the resolution.
Position resolution should **be better than 0.2mm**
Focus resolution should be **better than 0.4mm**

What about radiation damage?

- Most of the beam dose in the fibre is from operations (1.5 MGy/a) and not therapy (7 kGy/a). QA is only 10%. Change of procedure?
- Weekly QA done already for MWPC.
- Plan to exchange the mats regularly (6-12 months).



Line scan from mat put in the beam dump



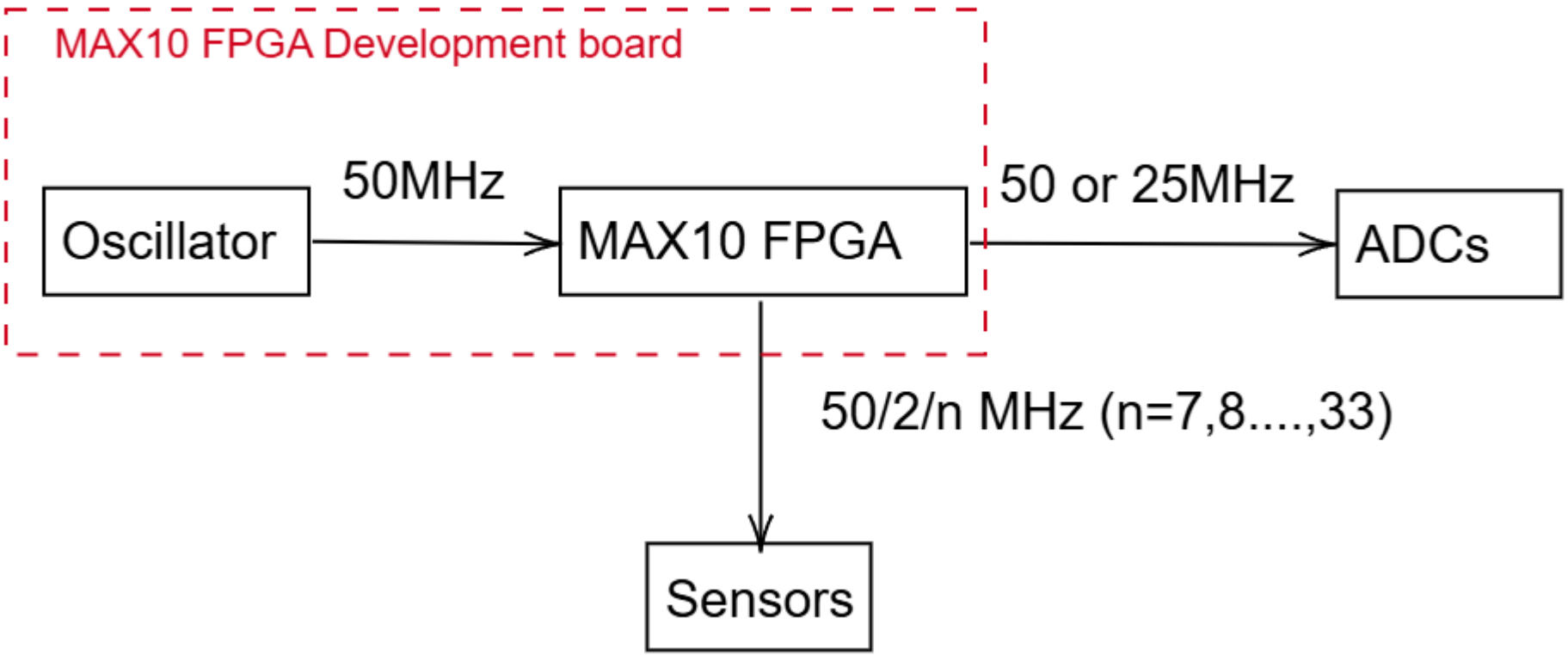
Area scan from mat put in the beam dump

- Backup and technical information:

How sensor and ADCs couple?

When sensor outputs video, ADC it.

Clock



Max sensor clock required by sensor and ADC: 4MHz;
Normally: n=7, sensor clock 3.57MHz; ADC clock 50 MHz;
n = 64, sensor clock 0.39MHz

ADC: AD7983 16-bit

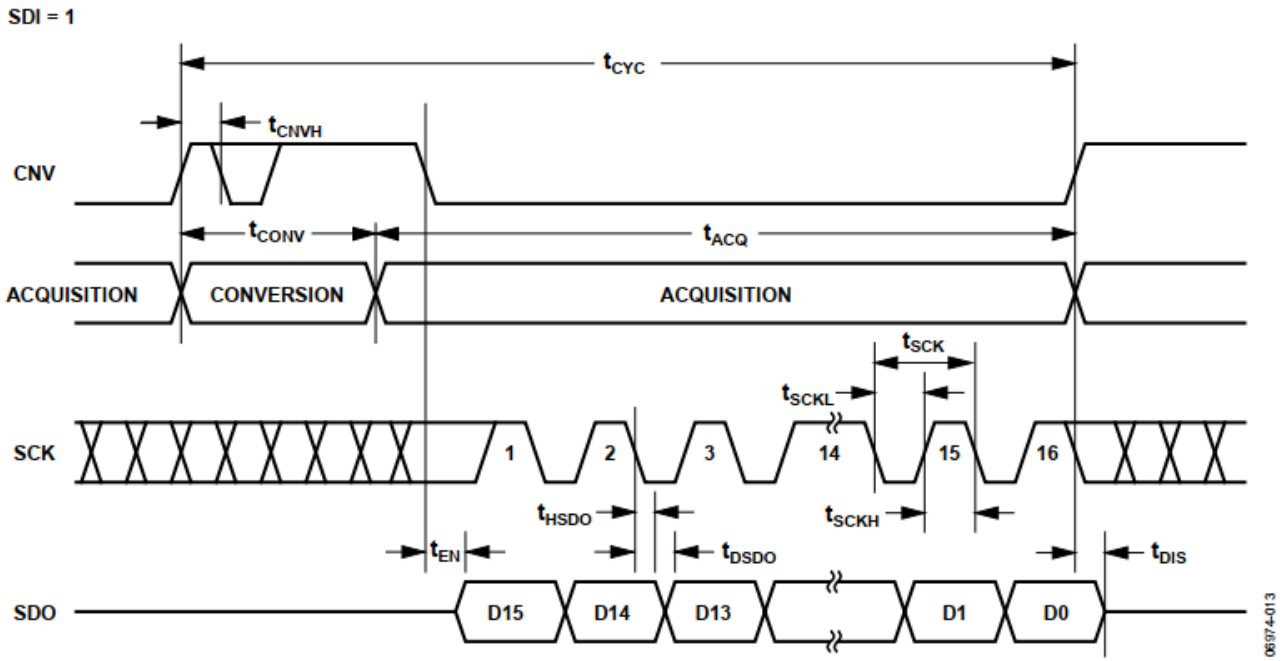
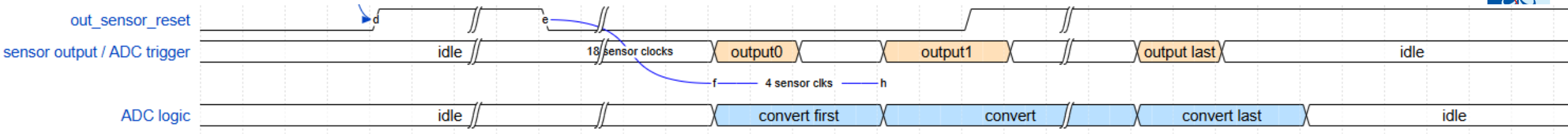


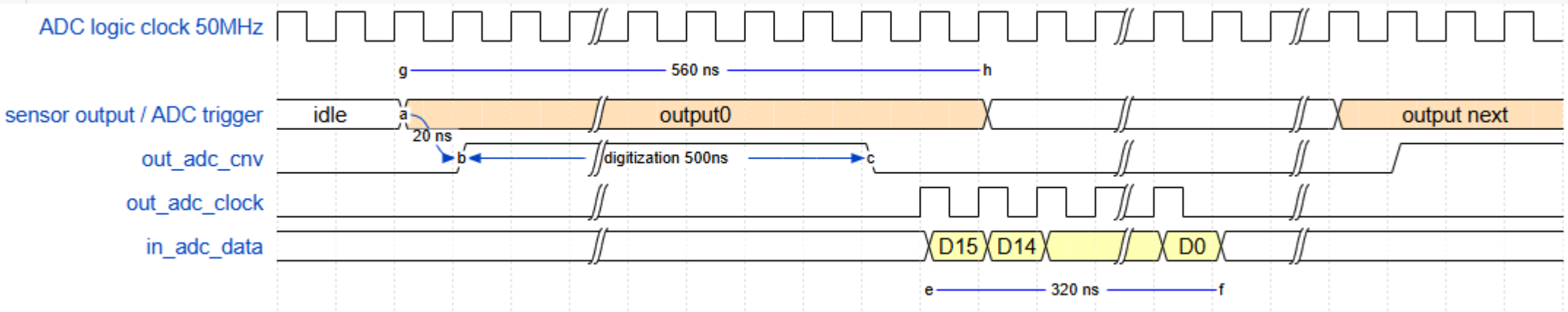
Figure 26. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing (SDI High)

ADC requires t_conv: min 300 ns, max 500 ns
FPGA provide CNV and SCK(ADC clock), receive SDO(ADC data)
FPGA settings: CNV > 500 ns
SCK 50MHz or 25MHz

Sensor and ADC



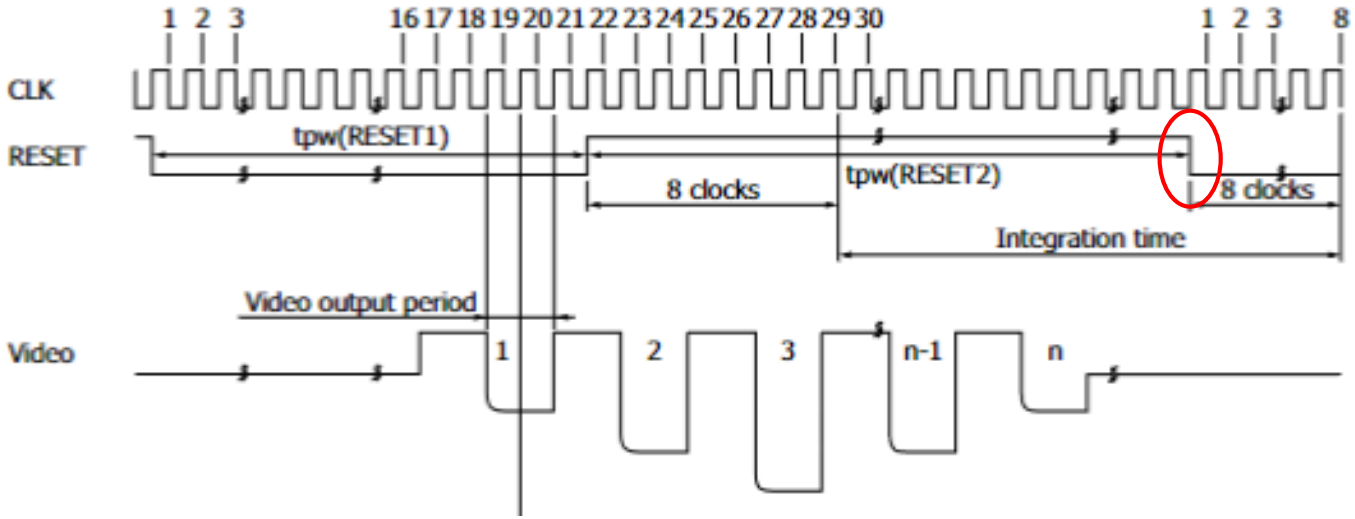
18 sensor clocks after sensor reset low, ADC logic is triggered;
then it is triggered every 4 sensor clocks until the last channel



ADC convert the video signal into digital data, and then FPGA acquires the 16-bit ADC data with 50 MHz ADC clock;

Integration time Range

Sensor RESET(Frame Clock) integration time



Sensor RESET is frame clock for one single board

New RESET low can only come after all channel read
For 64 channels, it is (18 + 64*4) sensor clocks = 76.7 μs
At least 21 RESET low is required
When sensor clock is 3.57 MHz

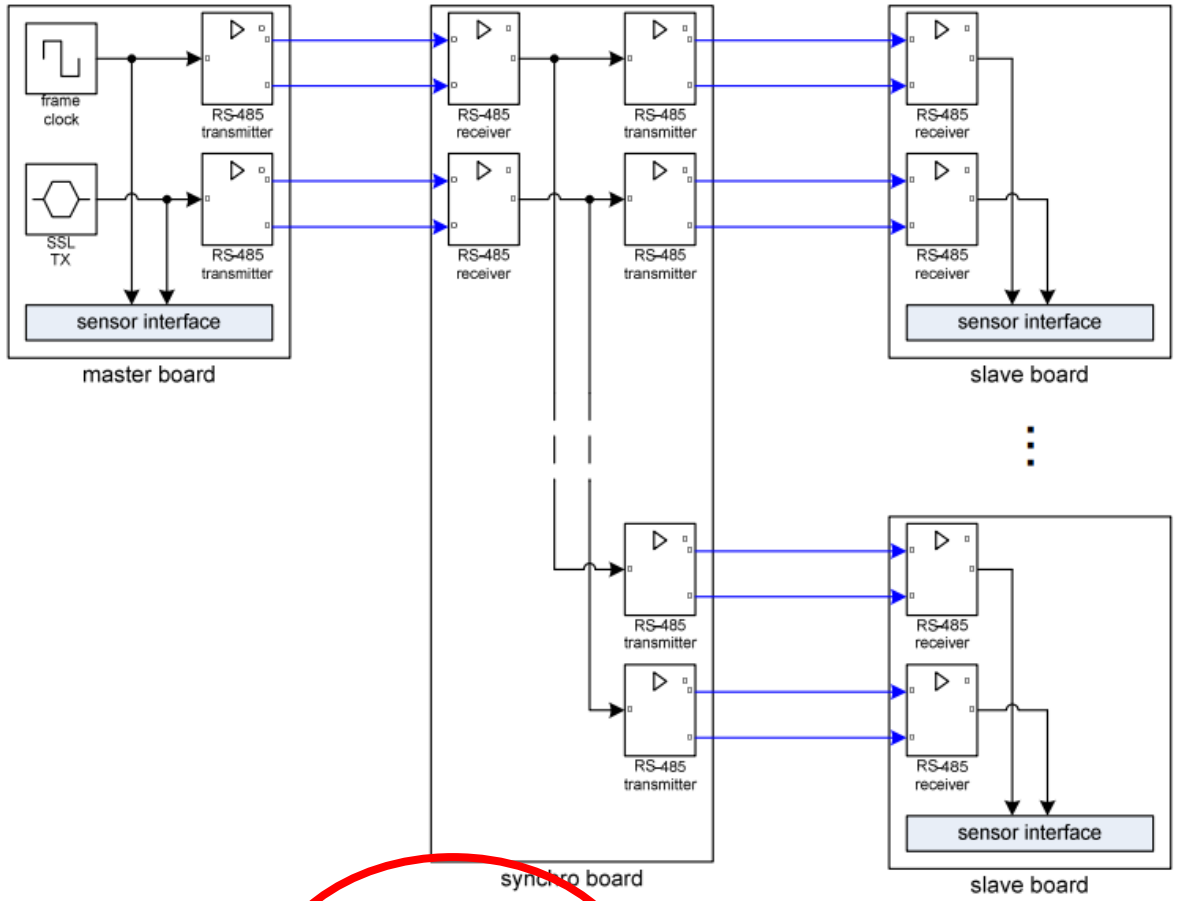
Max frame clock/ RESET rate: 21 RESET low + 253 RESET high **13 kHz ;**
integration time 70.9 μs

Min frame clock/ RESET rate : 21 RESET low + 4096 (12-bit counter) RESET high **0.86 kHz** ;
integration time 1.14 ms

(longer integration can be achieved by slowing down the sensor clock)

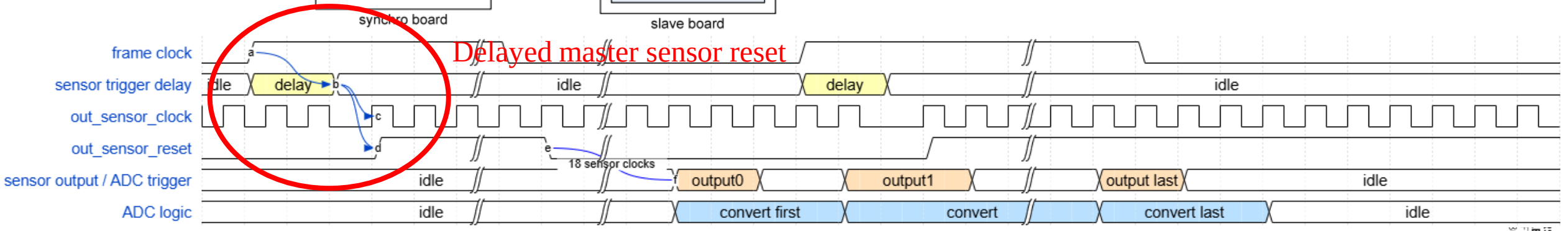
Synchronization

Synchronization



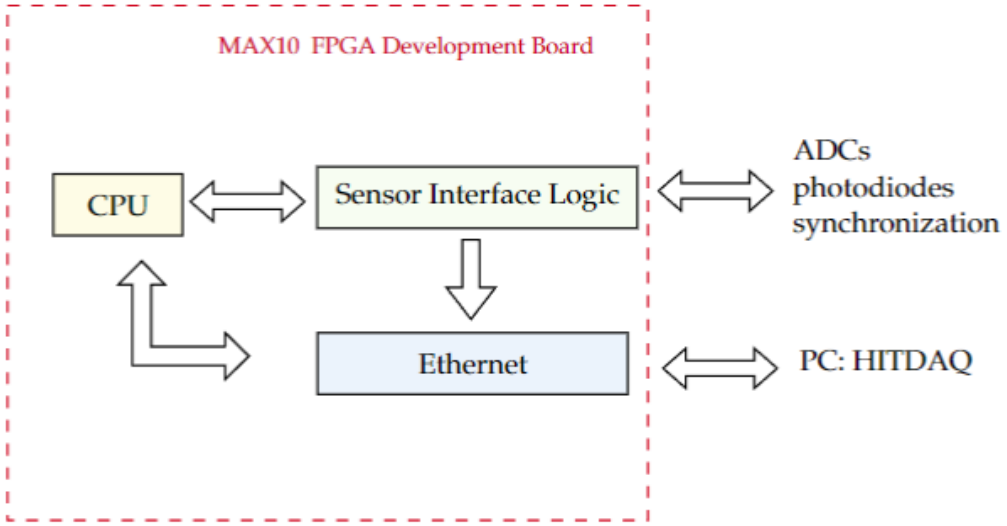
Frame clock and SSL(data with frameID) are sent from master board to slave board via synchro board;

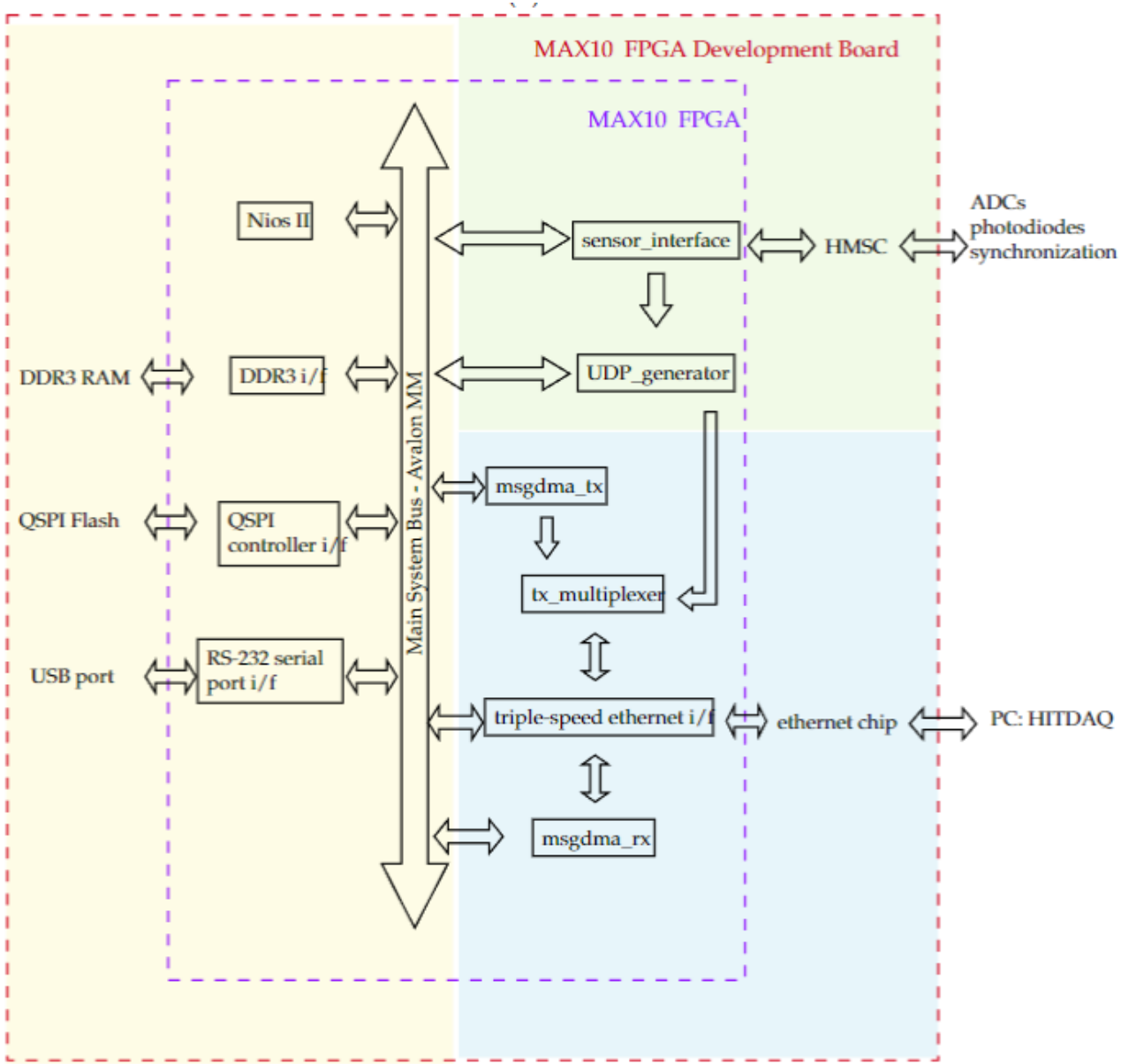
For slave board, the received frame clock is the sensor RESET.
For master board, the sensor RESET is the delayed frame clock.



Data Flow

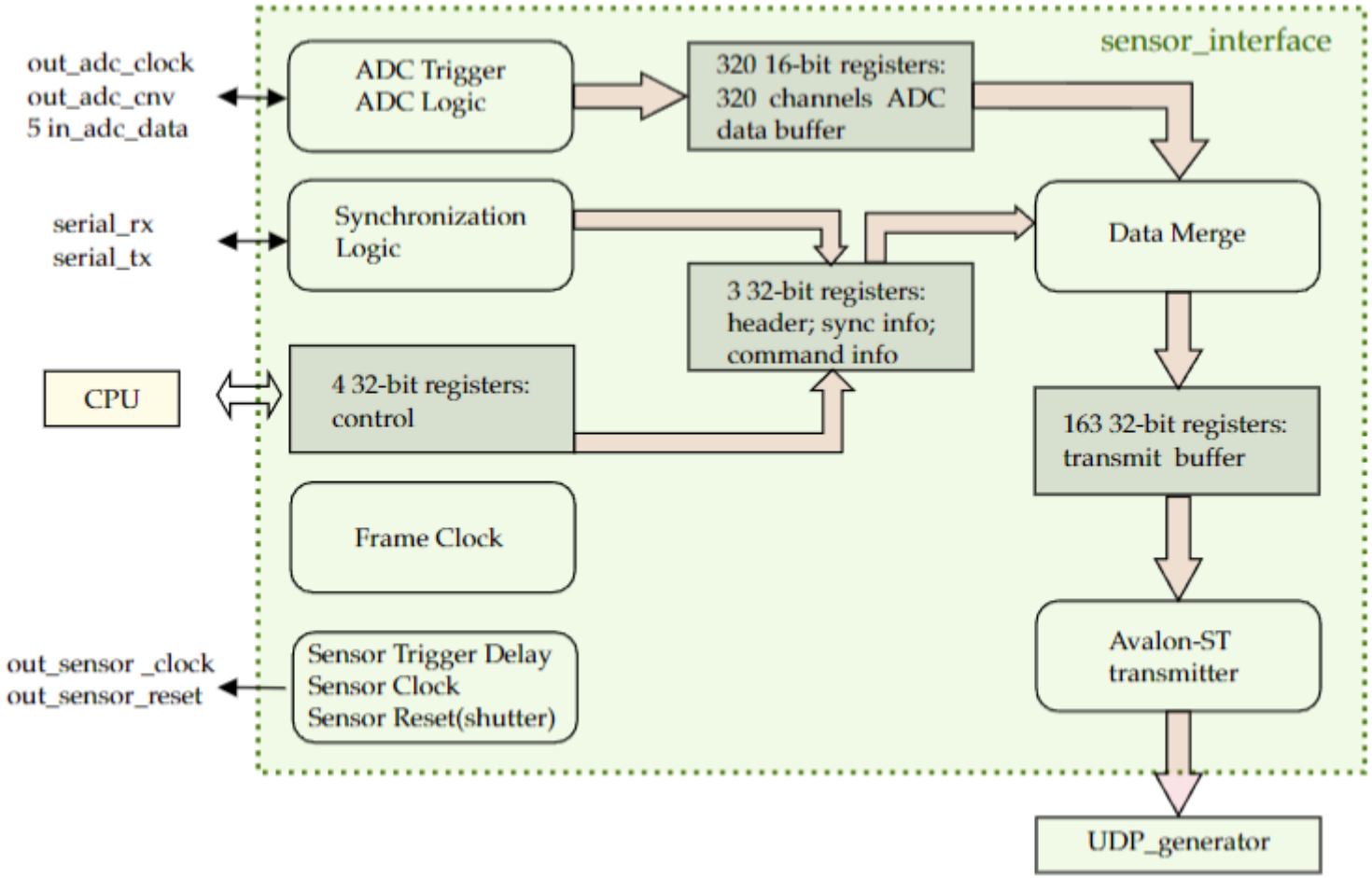
FPGA structure





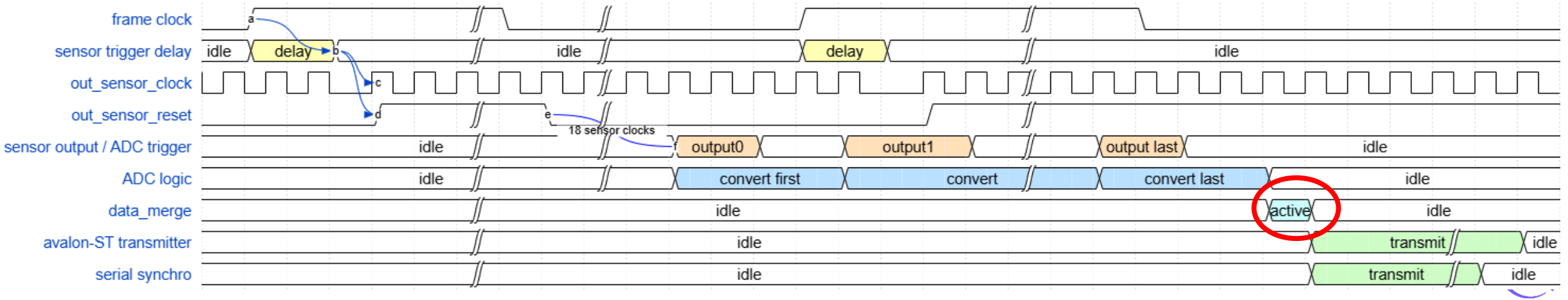
FPGA function: CPU + Ethernet interface + Sensor interface
HITDAQ talks to CPU, thus change sensor interface settings
Sensor_interface collects data sends to UDP_generator and than to ethernet

Sensor_interface logic blocks and data Flow



Sensor interface has several important registers.
ADC Logic block collect 5*64 channel data and store it in ADC data buffer;
A 3 32-bit registers block store sync data from SSL and command info;
Data Merge logic merge these two blocks into one transmit buffer in one clock;
Avalon-ST transmitter streams out 163 32-bit data one by one

Sensor_interface



Once the last channel has been digitized, the data are merged and then transmitted.

Currently, the data is streamed to a block for reconstructing the position and sigma of beam and then together with the results to the UDP_generator.