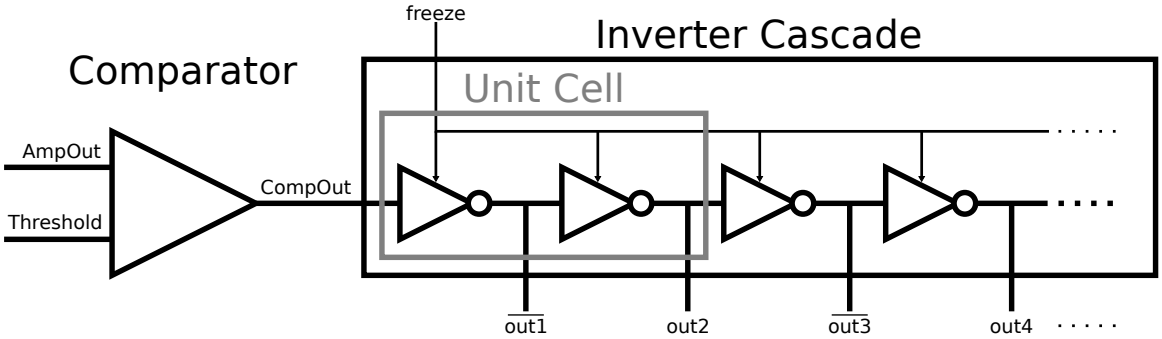
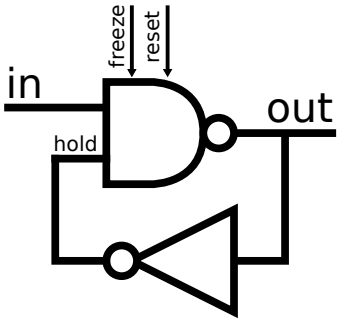
Goal

- highly precise timing (order of 100ps)
- simple to calibrate
- resilient to fluctuation in production and operation
- low power draw and space usage

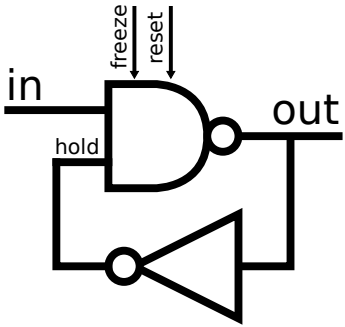
Overall Design Concept

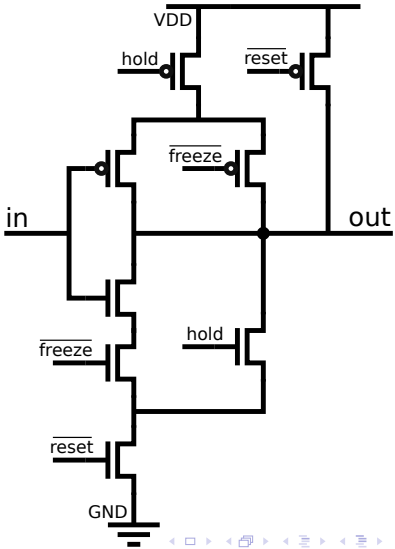


Latch Circuit



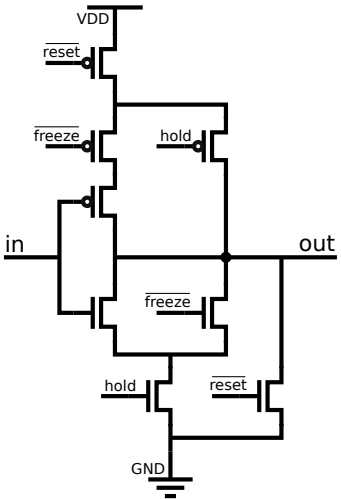
Latch Circuit for Active Low Signal





Latch Circuit for Active High Signal

- 3 PMOS transistors in a row
- therefore slower at same structure size
- can be compensated by tuning PMOS transistor width or NMOS transistor length in AL circuit



Symmetrical versus Asymmetrical Topology

Asymmetrical Circuit

- fewer components
- no tuning required

Symmetrical Circuit

- AH and AL circuits are not identical
- therefore requires tuning in design phase or via a DAC setting

Inline versus Branchoff Latch

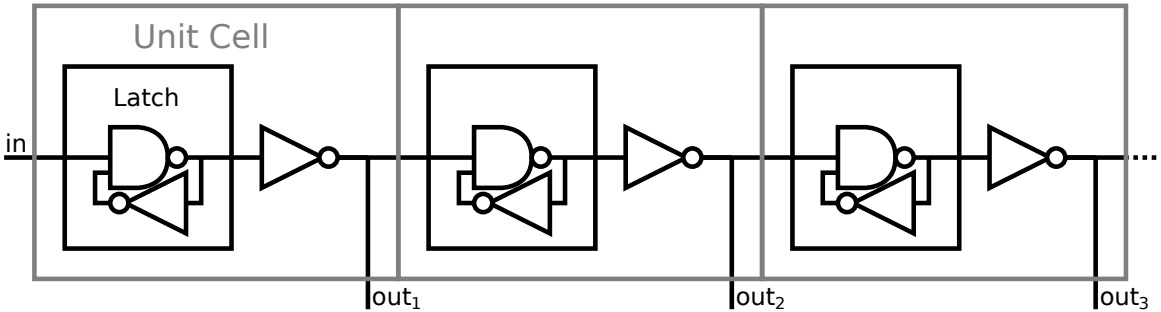
Inline

- fewer components
- no unnecessary inverter flips

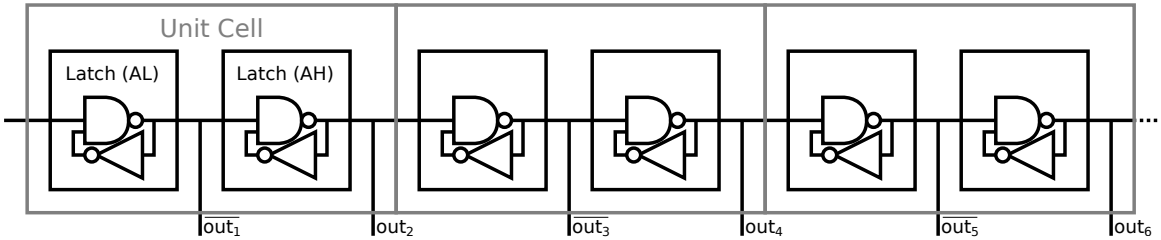
Branchoff

- slower latch circuit is out of the critical path
- readout load is also not in the critical path
- therefore much faster

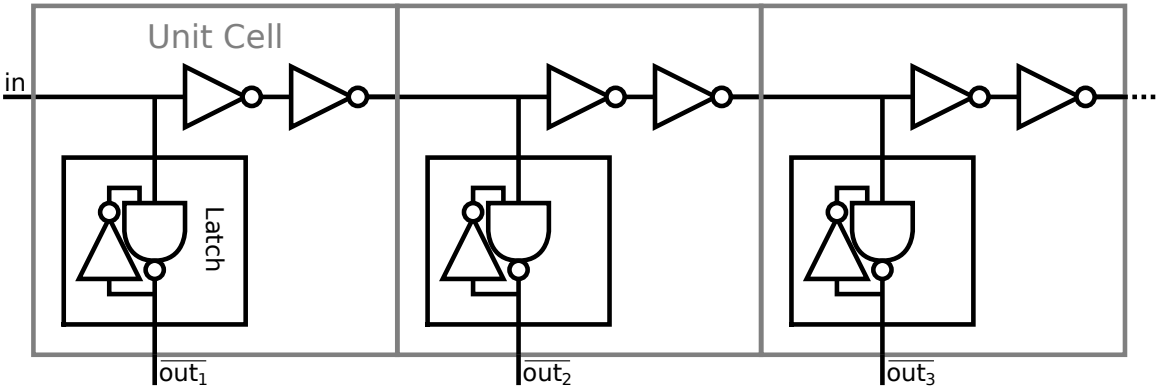
Inline Asymmetric



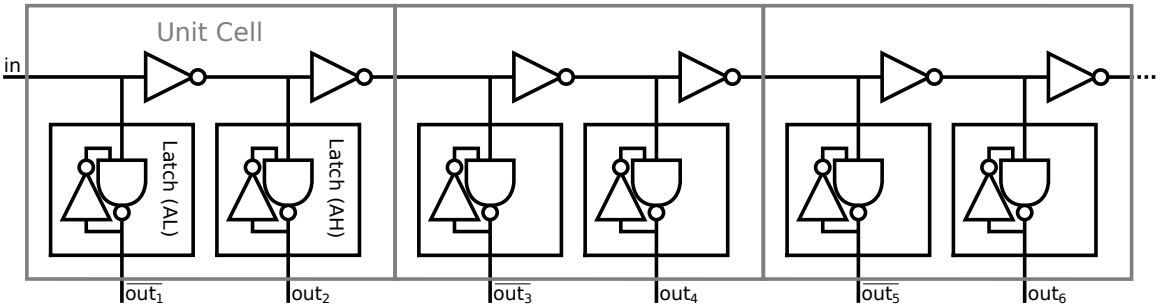
Inline Symmetric



Branchoff Asymmetric



Branchoff Symmetric



Ring Topology