Goals

- generate a reference signal (freeze)
- sharply defined timing relation to clock signal
- if possible, keep delay low

Symmetrical versus Asymmetrical Topology

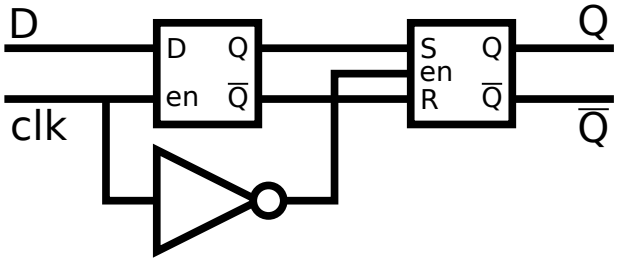
synchronous start, asynchronous stop

- not jitter issues
- no calibration required
- issues with input timing around clock edge
- inefficient: timer must be activated every clock cycle

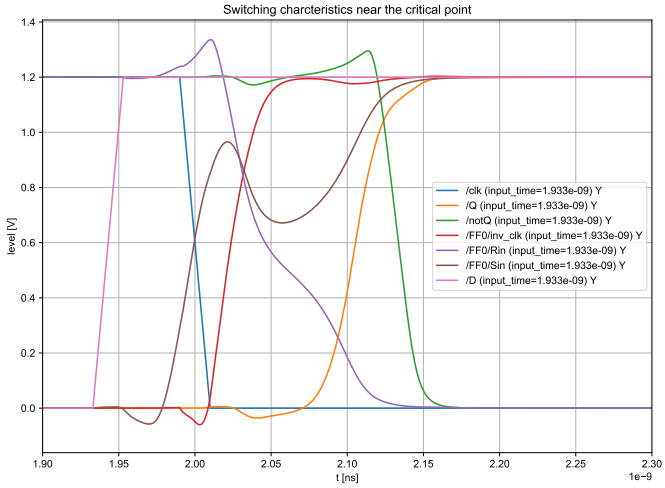
asynchronous start, synchronous stop

- jitter issues likely
- possible issues with short signals (*tot* lower than a clock cycle)
- preferred since energy efficient

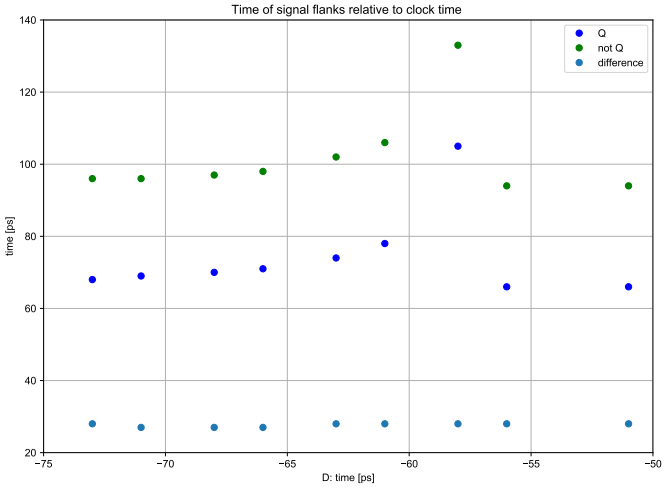
Master-Slave D-Flipflop (falling edge triggered)



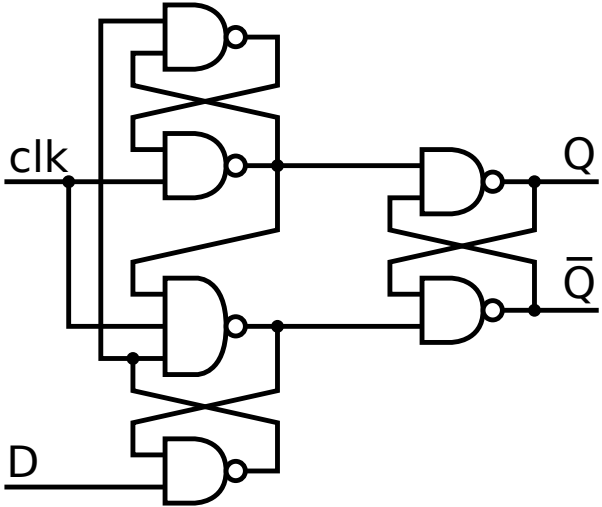
Understanding Metastability



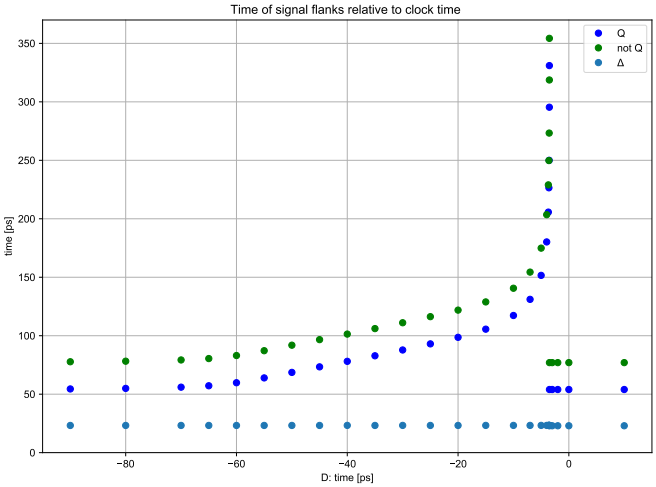
Jitter from Setup Time Violation



Classical D-Flipflop (rising edge triggered)

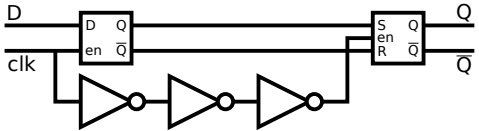


Jitter Classical D-Flipflop

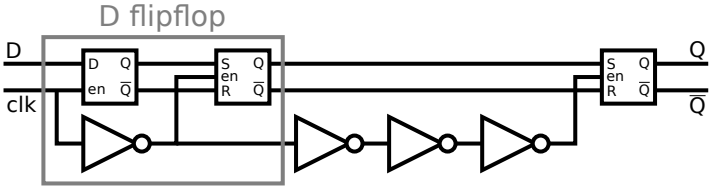


Compensation Strategies

Delayed Switching



Additional Latch



Effect of Compensation Strategies