

# Evaluating stretched TDC: Status Update

Alexander Schmidt

21. August 2022

# Contents

1 Introduction

2 Results

3 Outlook

# 1. Reminder: Stretched TDC Circuit

# The goal

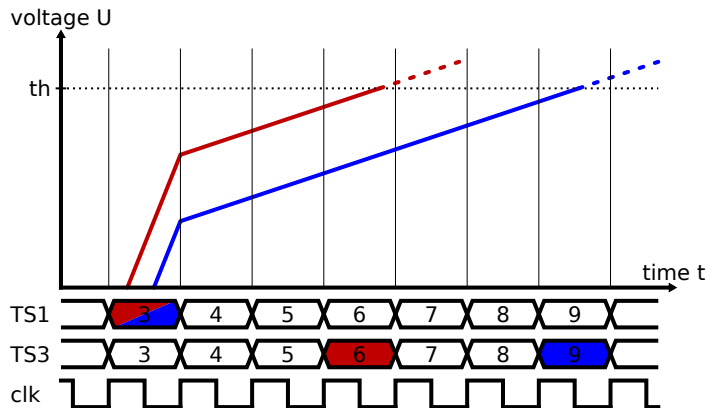
We want to measure particles

- improve precision of time measurements for hits
- that's it

# Performance Metrics

- precise timing (ideally below 1ns)
- homogenous time resolution
- low variance between pixels
- try to keep power draw low if possible

# Idea: Stretched TDC

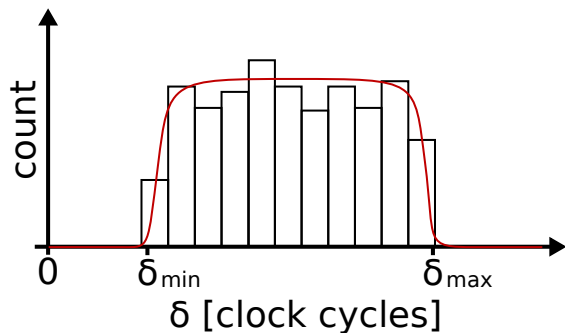


# Expected outcome for the distribution of $\delta$

- $TS3$  should have a delay from  $TS1$  which distributed approximately evenly over a sharply defined range
- define  $\delta := TS3 - TS1$
- define  $\delta_{min}$  and  $\delta_{max}$  as the edges of the distribution
- reconstruct  

$$t_{hit} = clock\_period \cdot (TS1 + \frac{\delta - \delta_{min}}{\delta_{max} - \delta_{min}})$$

Expected distribution of  $\delta$  over all hits



# Fit the delta Distribution

- A box function might sound natural but fits will likely fail due to the unsteady nature
- Instead as sigmoid function to approximate the edges of the block
- $\text{sig}(x; c, s) := \frac{1}{1 + \exp(-4s(x - c))}$
- free parameters: edge position  $c$  and slope  $s$
- full fit function: multiply two sigmoids  

$$f(x; A, B, l, r, s_l, s_r) := B + A \cdot \text{sig}(x; l, \frac{s_l}{A}) \cdot \text{sig}(x; r, \frac{s_r}{A})$$

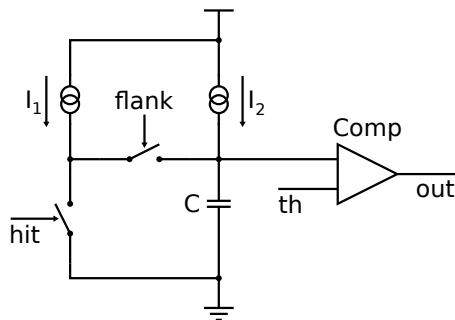
Sigmoid curve and full fit function  
missing :)



# Implementation: Stretched TDC circuit

- By default pull voltage at the capacitor to *GND*
- Once a hit is registered, disconnect the connection to ground such that the current supplies  $I_1$  and  $I_2$  charge the capacitor
- Once the clock edge hits, disconnect  $I_1$ , such that now only  $I_2$  charges the capacitor
- Once the threshold is passed, store the current value of *TS3*

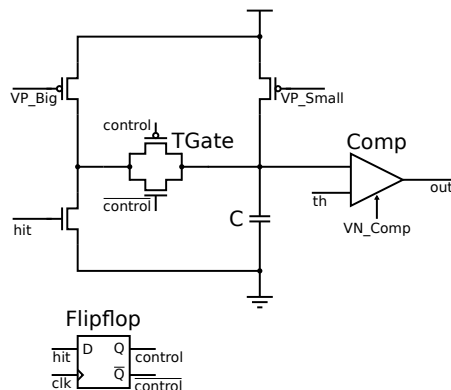
Simplified model of the *stretched TDC* circuit



# Implementation: Stretched TDC circuit

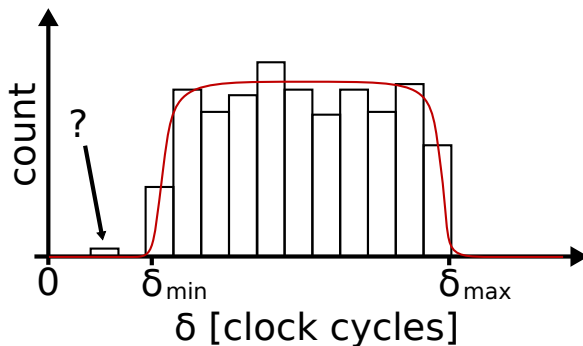
- For current source use pmos transistors in saturation, control the current with DAC values ( $VP\_Big$  and  $VP\_Small$ )
- The connection to ground is regulated using an NMOS transistor
- The connection of  $I_1$  to the capacitor is regulated using a transmission gate
- Use a Flipflop for the transmission gate input, such that is changed once the clock edge hits but only if a hit is there
- Two more DAC values for *threshold* and  $VN\_Comp$

Transistor level model of the *stretched TDC* circuit



## Problem: Stray values for $\delta$

How do we interpret timestamps with delta outside the range  $[\delta_{\min}, \delta_{\max}]$ ?



Depends on what the cause is...

# Problem: Manufacturing variance

- There is some pixel-by-pixel variance in transistor parameters and (more importantly)  $C$
- We need to individually find  $\delta_{max}$  and  $\delta_{min}$  for each pixel to calibrate the time reconstruction

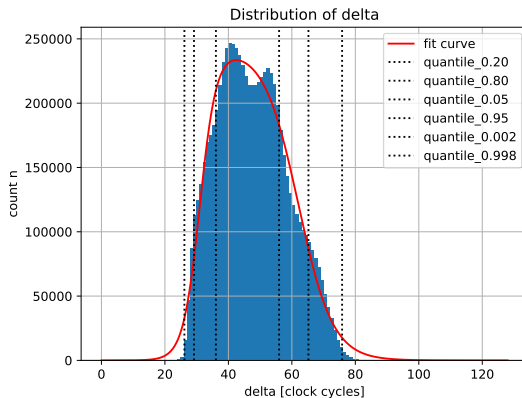
## 2. Results: Stretched TDC Analysis

# Measurement setup

- I did runs for a lot of parametric selections, but for now look at just 2 of them
- Slow and precise:  $VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300\text{mV}$
- Fast and tight  $VP\_Big = a$ ,  $VP\_Small = c$ ,  $VN\_Comp = a$ ,  $th = 1300\text{mV}$

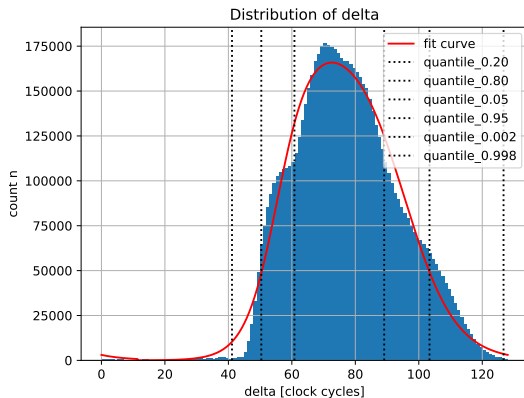
# Global delta distribution

$VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



# Global delta distribution

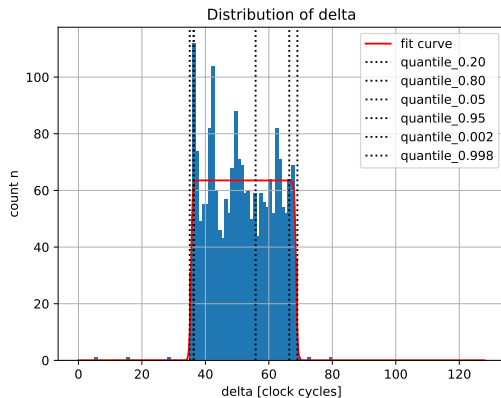
$$VP\_Big = a, VP\_Small = c, VN\_Comp = a, th = 1300mV$$





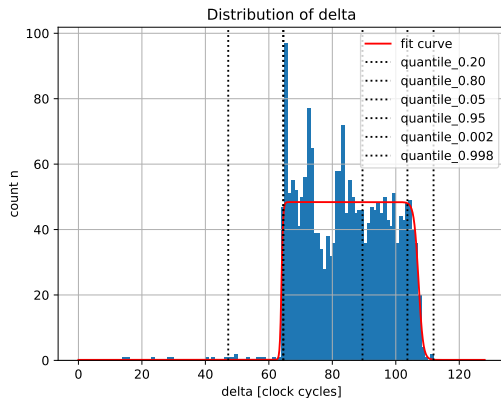
# Single Pixel delta distribution

$$VP\_Big = 8, VP\_Small = 8, VN\_Comp = a, th = 1300mV$$



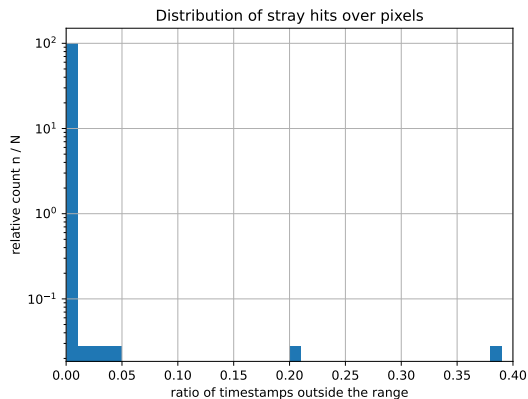
# Single Pixel delta distribution

$$VP\_Big = a, VP\_Small = c, VN\_Comp = a, th = 1300mV$$



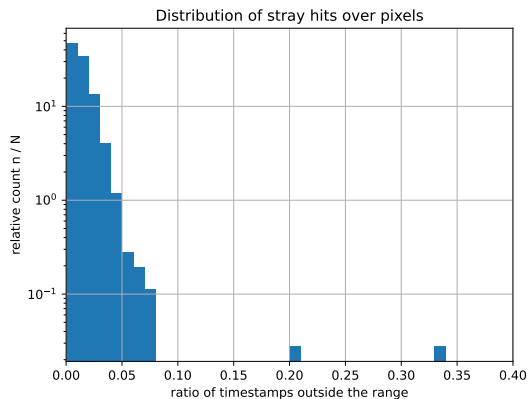
# How many stray timestamps are there?

$$VP\_Big = 8, VP\_Small = 8, VN\_Comp = a, th = 1300\text{mV}$$



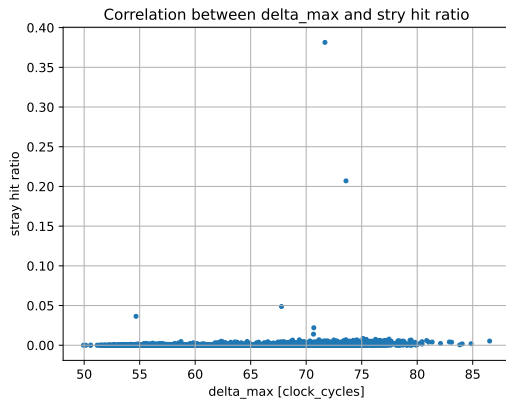
# How many stray timestamps are there?

$$VP\_Big = a, VP\_Small = c, VN\_Comp = a, th = 1300mV$$



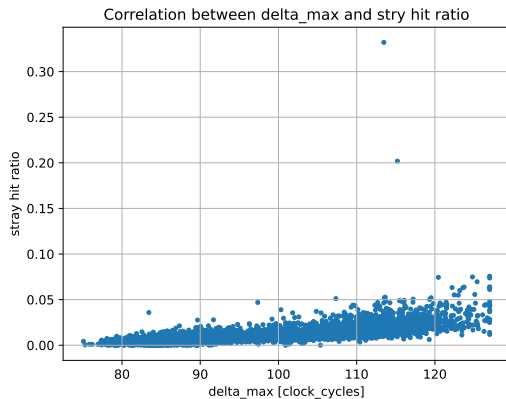
# Do stray timestamps correlate with $\delta_{max}$ ?

$VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



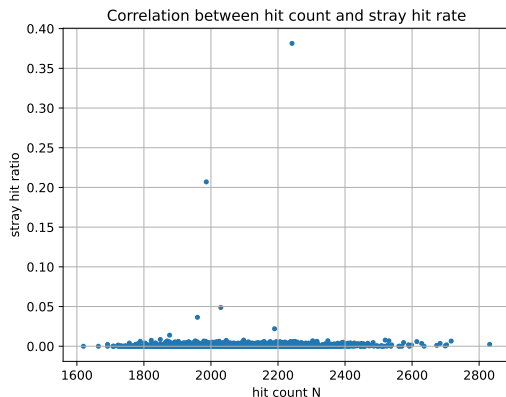
# Do stray timestamps correlate with $\delta_{max}$ ?

$VP\_Big = a$ ,  $VP\_Small = c$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



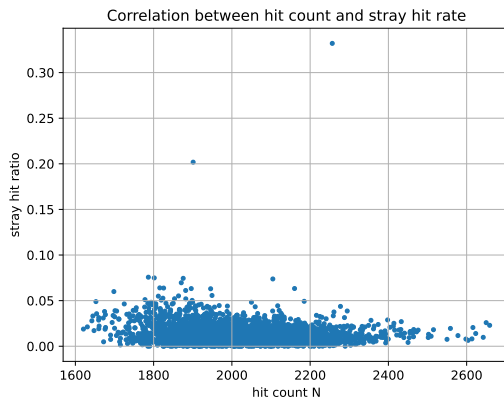
# Do stray timestamps correlate with amount of hits (hot or dead pixels)?

$$VP\_Big = 8, VP\_Small = 8, VN\_Comp = a, th = 1300mV$$



# Do stray timestamps correlate with amount of hits (hot or dead pixels)?

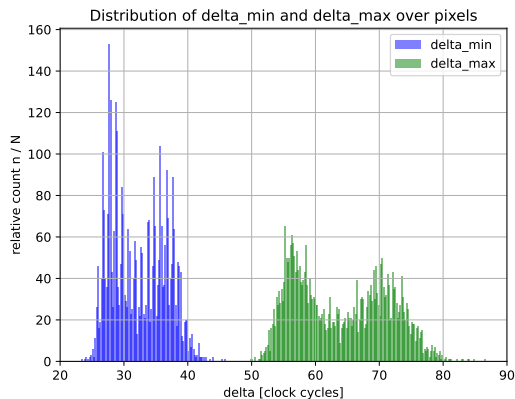
$$VP\_Big = a, VP\_Small = c, VN\_Comp = a, th = 1300mV$$





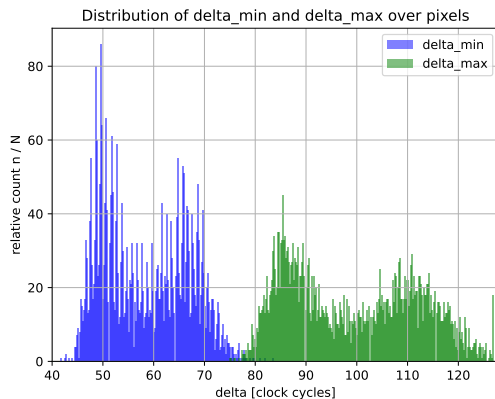
# Distribution of $\delta_{max}$ and $\delta_{min}$ over all pixels

$VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



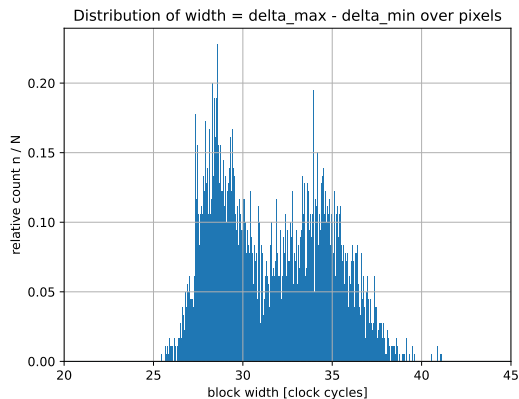
# Distribution of $\delta_{max}$ and $\delta_{min}$ over all pixels

$$VP\_Big = a, VP\_Small = c, VN\_Comp = a, th = 1300mV$$



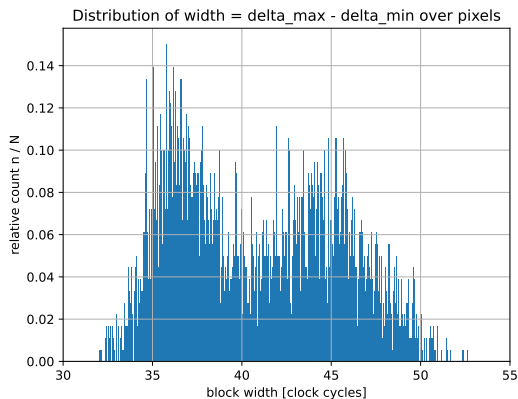
# Distribution of block width $w := \delta_{max} - \delta_{min}$ over all pixels

$VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



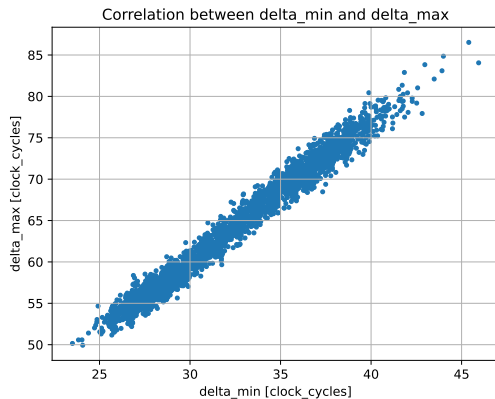
# Distribution of block width $w := \delta_{max} - \delta_{min}$ over all pixels

$VP\_Big = a$ ,  $VP\_Small = c$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



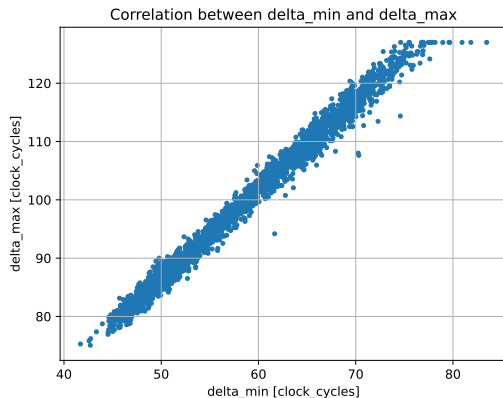
How does  $\delta_{max}$  relate to  $\delta_{min}$ ?

$VP\_Big = 8$ ,  $VP\_Small = 8$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



How does  $\delta_{max}$  relate to  $\delta_{min}$ ?

$VP\_Big = a$ ,  $VP\_Small = c$ ,  $VN\_Comp = a$ ,  $th = 1300mV$



# Up next

- See if there is correlation of fit results with pixel position on the chip (row, col)
- Do parametric analysis for DAC values
- Find the source of stray timestamps
- Find out which part of the circuit is influenced the most by manufacturing variance (I assume it is C)
- Any suggestions?