Evaluating stretched TDC: Status Update

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1. September 2022

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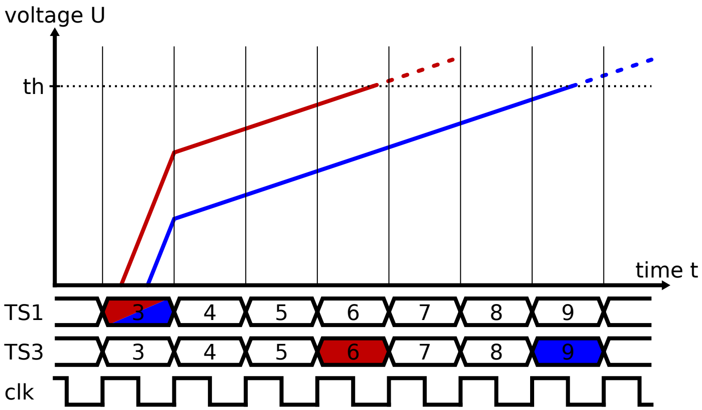
1. Theoretical Analysis of *Stretched TDC* Circuit

Reminder: Stretched TDC Concept



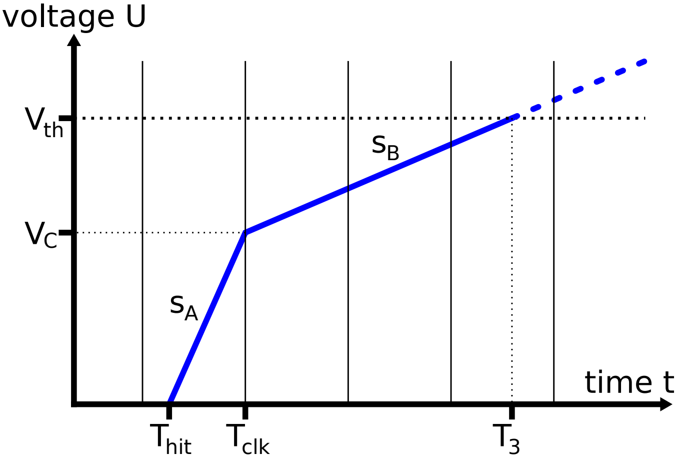
Charging Slope Analysis: dependence of δ on T_hit

$$s_A = \frac{V_C}{T_{clk} - T_{hit}}$$

$$s_B = \frac{V_{th} - V_C}{T_3 - T_{clk}}$$

$$V_C = s_A \left(T_{clk} - T_{hit} \right)$$

$$\begin{aligned} \delta \equiv T_3 - T_{clk} &= \frac{V_{th} - V_C}{s_B} \\ &= \frac{V_{th}}{s_B} - \frac{s_A}{s_B} \left(T_{clk} - T_{hit} \right) \\ &= -\frac{s_A}{s_B} \left(T_{clk} - T_{hit} \right) + const. \end{aligned}$$



Charging Slope Analysis: δ_{min}, δ_{max} and magnification

Earliest hit in clock period:

$$T_{hit} = T_{clk} - T$$

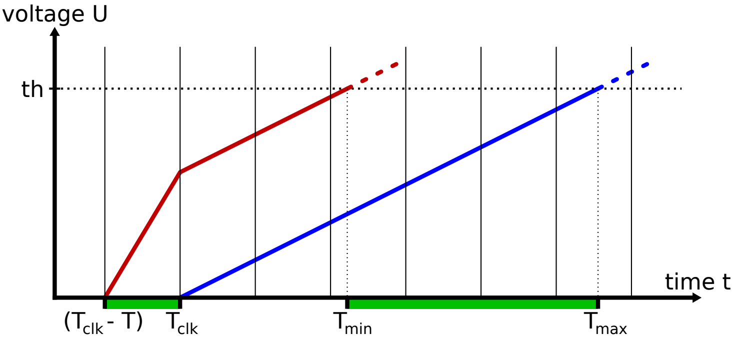
$$\Rightarrow \delta_{min} = \frac{s_A}{s_B} T + K$$

$$\boxed{\delta = -\frac{s_A}{s_B}\left(T_{clk} - T_{hit}\right) + K}$$

Latest hit:

$$T_{hit} = T_{clk}$$

$$\Rightarrow \delta_{max} = K$$



Width of delta distribution:

$$w := \delta_{max} - \delta_{min} = \frac{s_A}{s_B} T$$

Time magnification:

$$\boxed{\eta = \frac{T}{w} = \frac{s_B}{s_A}}$$

Relation Between Charging Current and Slope

$$U(t) = \frac{Q(t)}{C} = \frac{It}{C}$$

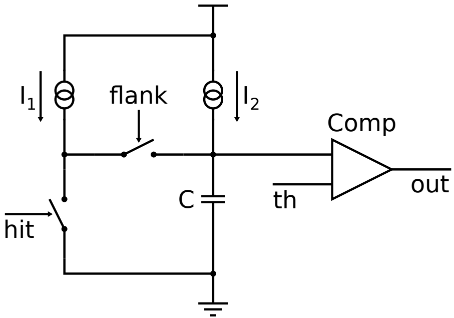
$$s := \frac{dU}{dt} = \frac{I}{C}$$

$$s_A = \frac{I_1 + I_2}{C}, \qquad s_B = \frac{I_2}{C}$$

Express the magnification in terms of I_1, I_2:

$$\boxed{\eta = \frac{s_B}{s_A} = \frac{I_2}{I_1 + I_2} = \frac{1}{1 + \frac{I_1}{I_2}}}$$

Stretched TDC circuit (simpified model)



Analysis of Pixel-by-Pixel variation

- We can analyse the variations in the ratio $\frac{I_2}{C}$ using $\frac{I_2}{C} = s_B$
- We can analyse the variations in the ratio $\frac{I_1}{I_2}$ using $\frac{I_1}{I_2} = \frac{1}{\eta} - 1$
- We *cannot* analyse the variations in I_1, I_2 or C individually since the observable circuit behaviour $U(t)$ is invariant under the transformation

$$\begin{aligned} \varphi : I_1 &\mapsto \alpha I_1 \\ I_2 &\mapsto \alpha I_2 \\ C &\mapsto \alpha C \end{aligned}$$

Evaluation pipeline

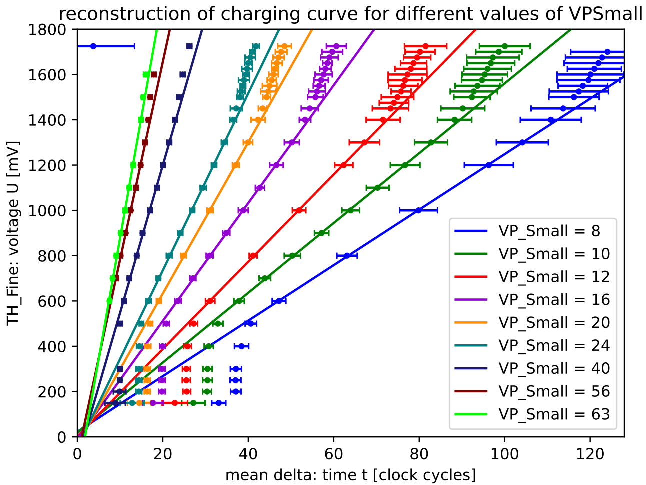
- take data with Sr90 source
- for each pixel calculate the distribution of delta values
- calculate $\overline{\delta}$, δ_{min} and δ_{max}
- analyse the dependence of results on DAC values and pixel position

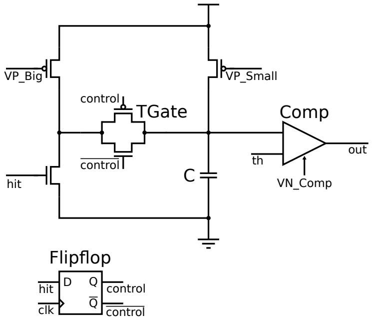
2. Reconstruction of the Charging Curve

Evaluation Methodology

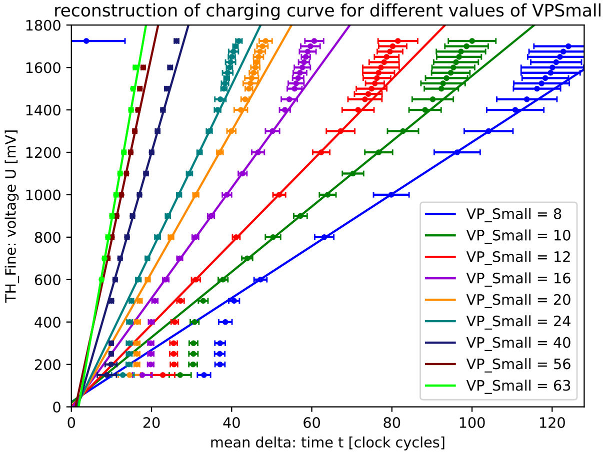
- Set $VP\_Big = 0$ in order to have a magnification of $\eta = 1$
- Take the mean δ for a series of thresholds
- The charging curve of C is just the inverse relation, $V(t) \equiv TH\_fine(\bar{\delta})$
- Fit a linear function. The slope is proportional to the charging current I_2

Reconstructed Charging Curve (Single Pixel)



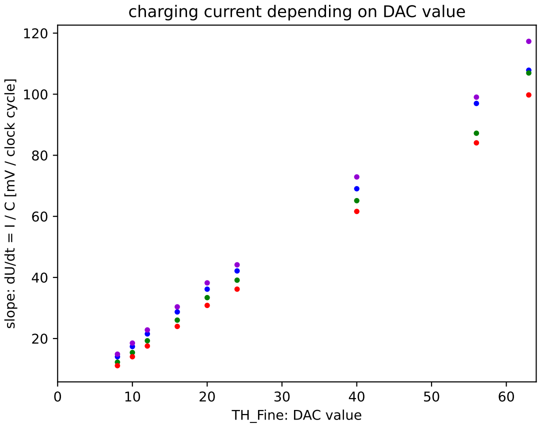


Charging Curve: Observations



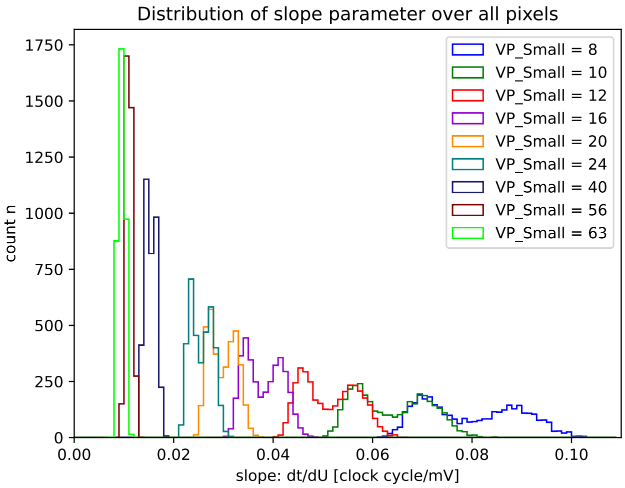
- linear region between 550mV and 1350mV (PMOS in saturation)
- nonlinearity above 1350mV as seen in simulation; likely due to transistor capacitance going down leaving saturation
- nonlinearity below 550mV; likely not from charging curve but from comparator being out of range
- fit curves meet near (0, 0) as expected

Current Characteristic of driver transistor (4 different pixels)

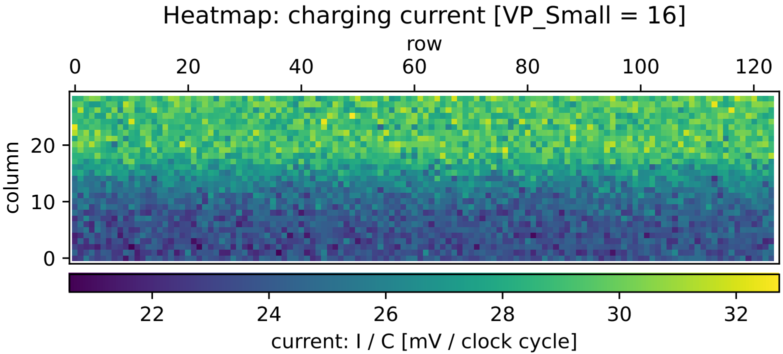


DACs seem to be tuned to be linear in current delivery.

Distribution of Charging Current over Pixels

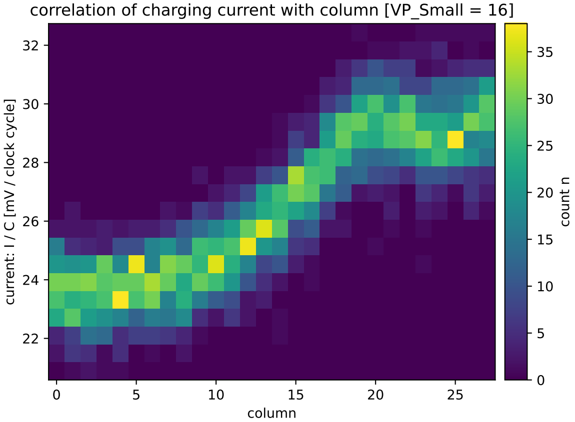


Dependence of Charging Current on Pixel Position



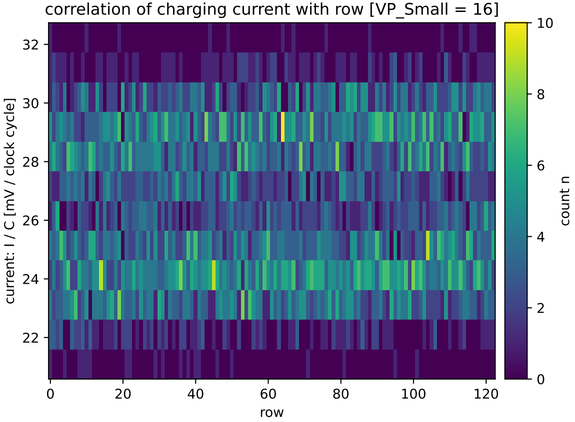
There seems to be a gradient over the column address (maybe power line resistance?)

Dependence of Charging Current on Column



This is less a smooth gradient and more a bimodal distribution. This is the likely explanation for the bimodality we have seen in many of the graphs.

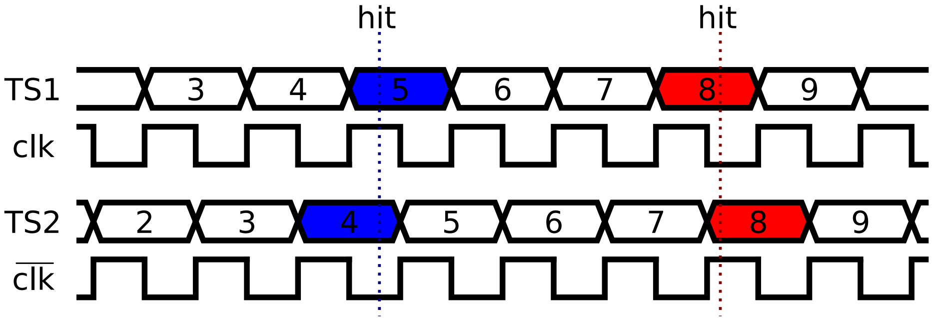
Dependence of Charging Current on Row



No noticable influence of row address.

3. Analysis of TS1 and TS2

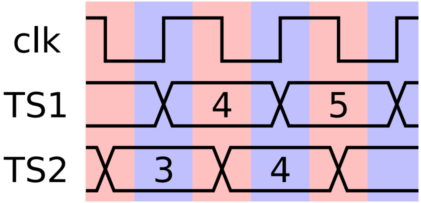
Concept: Phase Shifted Counters



- Improve time resolution using a second counter and an inverted (= shifted by 180°) clock
- TS2 given by the second counter should have the same value or one less than TS1
- If TS2 = TS1 - 1, the reconstructed time is in the first half of the clock cycle
- If TS2 = TS1, the reconstructed time is in the second half of the clock cycle

Gray Counter

- One the clock edges there is a short phase of instability when the timestamp switches
- In theory, you can use TS3 information to decide which timestamp is stable
- This only works if $\delta := ts3 - ts1$ and $\delta_{23} := ts3 - ts2$ are not significantly different
- Implement TS1 and TS2 as *gray counters* so that this issue does not arise



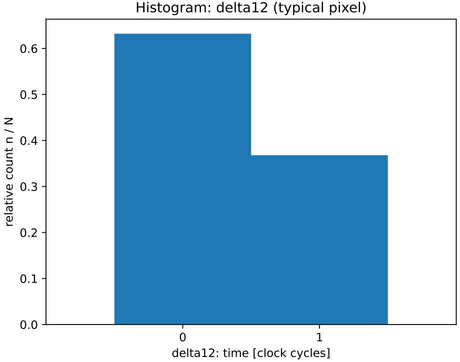
Half of a clock cycle (red), TS1 is stable and can be considered the definitive coarse timestamp. For the other half (blue), TS2 is stable.

Example: Gray Code

decimal	0	1	2	3	4	5	6	7	8	9	...
binary	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	...

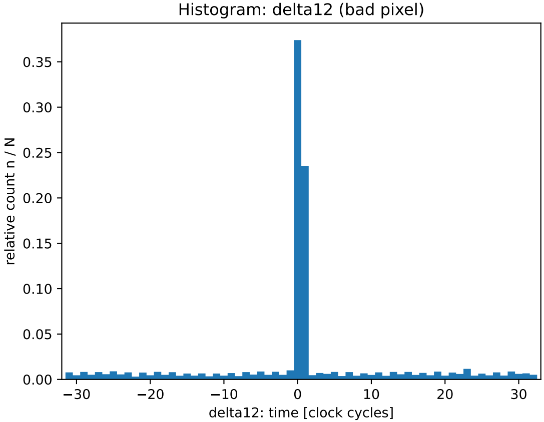
Histogram of δ_{12} for a typical pixel

According to theory, the difference $\delta_{12} := ts1 - ts2$ should have value $\delta_{12} = 0$ in 50% of the cases and $\delta_{12} = 1$ the other 50%. No other values should occur.



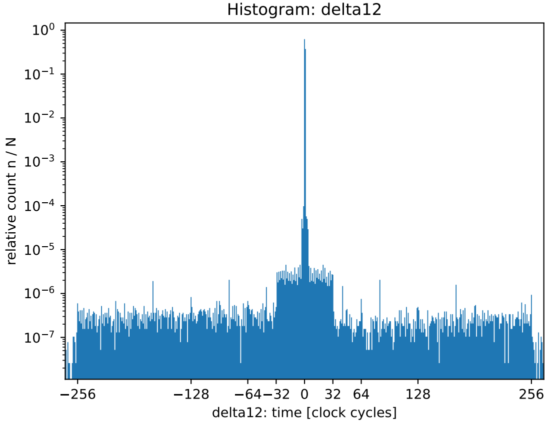
Not quite 50/50... But no *stray* values having $\delta_{12} \neq 0$.

Histogram of δ_{12} for the pixel with most stray values



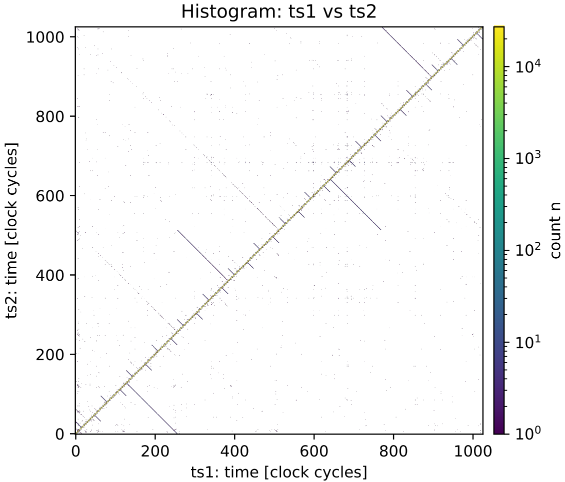
Around 40% of hits have $\delta_{12} \neq 0$. The distribution is ominous...

Histogram of δ_{12} globally



This block-shape may hint at individual bad bits in the gray counters.

Correlation between values of TS1 and TS2

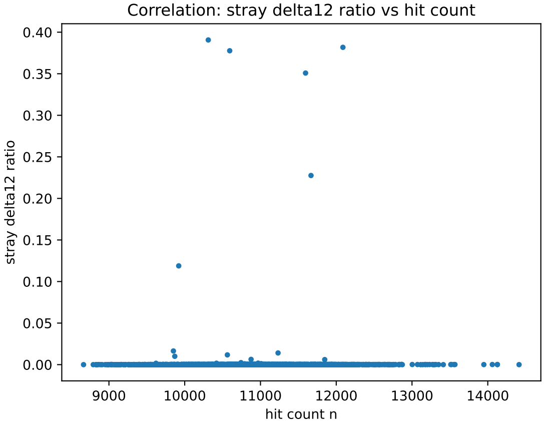


There are multiple noticeable accumulations.

- Starting at 2, in steps of 4 (length of diagonals 2; too small to see)
- Starting at 16, in steps of 32 (length of diagonals 16)
- Starting at 128, in steps of 256 (length of diagonals 128)
- Central diagonal at 512
- Faint diagonal at 256

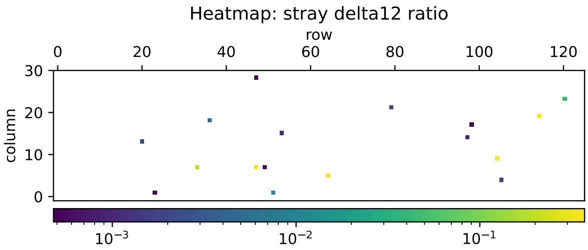
Is the ratio of stray δ_{12} correlated to hit rate?

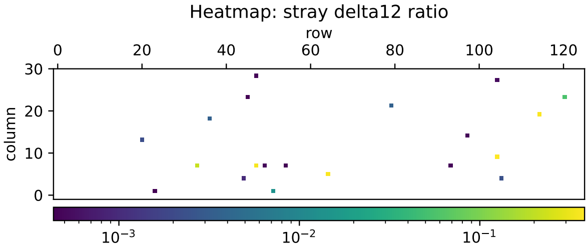
It might be hot pixels that produce bad timestamps.



But no.

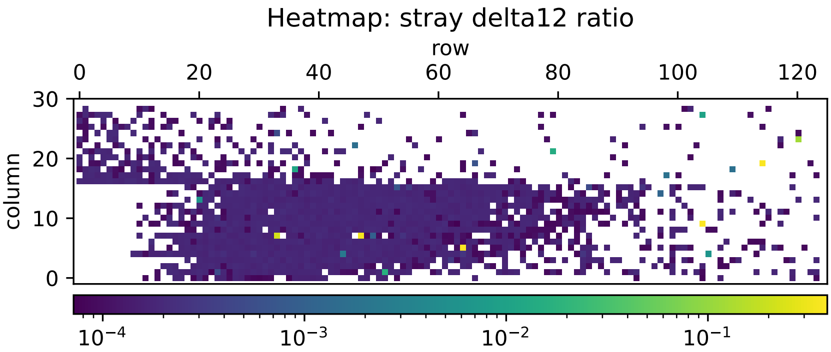
Where are the pixels with most stray δ_{12} values? (two different runs)





- no obvious pattern
- pixels with high rate of bad δ_{12} are the same between runs

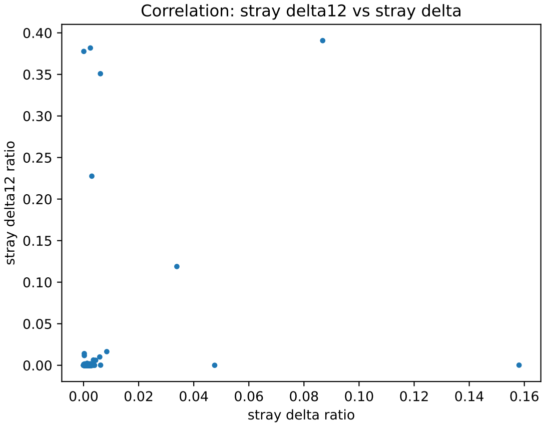
Where are the pixels with most stray δ_{12} values? (very long run)



Once again a split between high and low columns, but not that clear cut here.

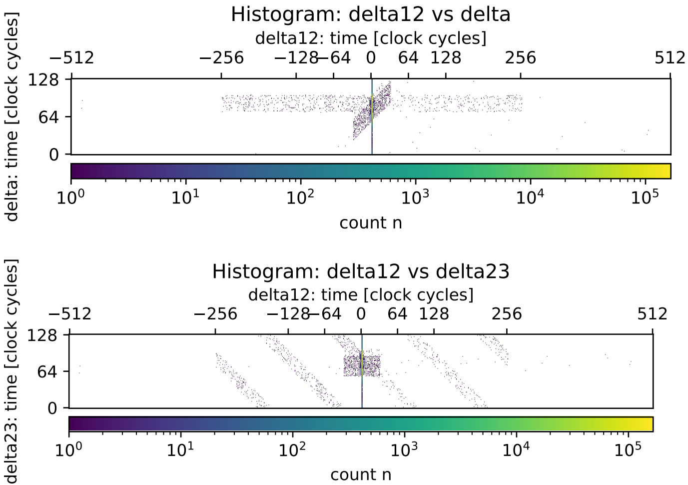
Is the ratio of stray δ_{12} correlated to the ratio of stray δ_{13}?

The the circuits for TS1, TS2 and TS3 might be broken in the same pixels.



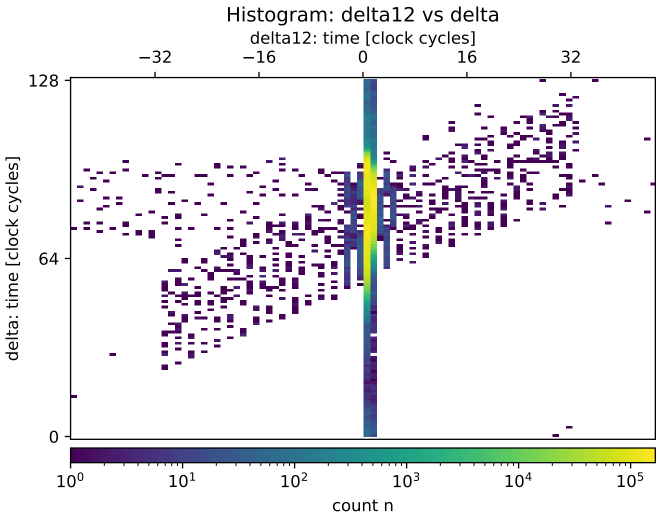
If there is a correlation, it is minor.

Correlation between δ_{12} and δ_{23}



- a horizontal block in δ_{13} likely means that TS2 is bad
- a horizontal block in δ_{23} likely means that TS1 is bad
- if the issue is due to instability in readout, the regions of unstable TS1 and unstable TS2 overlap significantly

Correlation between δ_{12} and δ_{13} or δ_{23} (zoomed in)



Up next

- Try a different chip to see if it shows a similar pattern
- Compare charging curve with simulation
- Have a look at the gray counter circuit
- Any suggestions?